SERIES
37XXXD
VECTOR NETWORK ANALYZER

MAINTENANCE MANUAL

Anritsu

490 JARVIS DRIVE | MORGAN HILL, CA 95037-2809

P/N: 10410-00264
REVISION: C
PRINTED: JULY 2007
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Anritsu's obligation covers repairing or replacing products which prove to be defective during the warranty period. Buyers shall prepay transportation charges for equipment returned to Anritsu for warranty repairs. Obligation is limited to the original purchaser. Anritsu is not liable for consequential damages.

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Updates to this manual, if any, may be downloaded from the Anritsu Internet site at:
http://www.us.anritsu.com

DECLARATION OF CONFORMITY

Manufacturer's Name: ANRITSU COMPANY

Manufacturer's Address: Microwave Measurements Division
490 Jarvis Drive
Morgan Hill, CA 95037-2809
USA

declares that the product specified below:

Product Name: Vector Network Analyzer

Model Number: 37247D,37269D,37277D,37297D,37347D,37369D,37377D,37397D

conforms to the requirement of:

EMC Directive 89/336/EEC as amended by Council Directive 92/31/EEC & 93/68/EEC
Low Voltage Directive 73/23/EEC as amended by Council directive 93/68/EEC

Electromagnetic Interference:

Emissions: CISPR 11:1990/EN55011:1991 Group 1 Class A

Immunity:
EN 61000-4-2:1995/EN50082-1:1997 - 4kV CD, 8kV AD
EN 61000-4-3:1997/EN50082-1:1997 - 3V/m
ENV 50204/EN50082-1:1997 – 3V/m
EN 61000-4-4:1995/EN50082-1:1997 - 0.5kV SL, 1kV PL
EN 61000-4-5:1995/EN50082-1: 1997 - 1kV L-L, 2kV L-E
EN 61000-4-6:1994/EN61326: 1998 – 3V
EN 61000-4-11:1994/EN61326: 1998 – 1 cycle@100%

Electrical Safety Requirement:

Product Safety: EN 61010-1:2001

Corporate Quality Director

Morgan Hill, CA

30 Sept 2004
Date

European Contact: For Anritsu product EMC & LVD information, contact Anritsu LTD, Rutherford Close, Stevenage Herts, SG1 2EF UK, (FAX 44-1438-740202)

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Chapter 1
General Information

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Figure 1-1. *Series 37XXXD Vector Network Analyzer System*

Chapter 1
General Information

1-1 SCOPE OF MANUAL

This manual provides general service and preventive maintenance information for the Anritsu 37XXXD models of Vector Network Analyzer (VNA) systems. It contains procedures for:

- Testing the instrument for proper operation.
- Verifying measurement accuracy and traceability to National Institute of Standards and Technology (NIST).
- Troubleshooting a failed instrument to the exchange subassembly level or the subsystem requiring adjustment.
- Adjusting instrument internal sub-systems.
- Locating and replacing failed parts.

Throughout this manual, the terms “37XXXD” and “VNA” will be used interchangeably to refer to all Models of the 37000D series VNA, unless otherwise noted.

1-2 INTRODUCTION

This chapter provides a general description of VNA systems, system serial numbers, frequency ranges, and related manuals. It also includes service strategy, available service facilities, and static-sensitive component handling precautions, and a list of recommended test equipment.

1-3 IDENTIFICATION NUMBER

All Anritsu instruments are assigned a six-digit ID number, such as “042503”. This number appears on a decal affixed to the rear panel. Please use this identification number during any correspondence with Anritsu Customer Service about this instrument.

1-4 ONLINE MANUAL

This manual is available for download as an Adobe Acrobat™ (*.pdf) file. The file can be viewed using Acrobat Reader™, a free program that is available from Adobe. This file is “linked” such that the viewer can choose a topic to view from the displayed “bookmark” list and “jump” to the manual page on which the topic resides. The text can also be word-searched. Updates to this manual, if any, may also be downloaded from the documents area of the Anritsu Internet site at: *http://www.us.anritsu.com*

1-5 SYSTEM DESCRIPTION

The 37XXXD Analyzers are microprocessor controlled Vector Network Analyzers. Each is a single-instrument system that contains a built-in signal source, a test set, and an analyzer subsystem. These analyzers are produced in eight models that cover a range of from 40 MHz to 65 GHz. The table below lists the frequencies for each model:

37XXXD Models and Frequency Ranges

Model	Freq Range	Model	Freq Range
37247D	40.0 MHz to 20.0 GHz	37347D	40.0 MHz to 20.0 GHz
37269D	40.0 MHz to 40.0 GHz	37369D	40.0 MHz to 40.0 GHz
37277D	40.0 MHz to 50.0 GHz	37377D	40.0 MHz to 50.0 GHz
37297D	40.0 MHz to 65.0 GHz	37397D	40.0 MHz to 65.0 GHz

1-6 RELATED MANUALS

The 37XXXD Vector Network Analyzer Operation Manual (10410-00261) describes the front panel operation for all 37XXXD models. It also contains general information, specifications, and Performance Verification procedures for all models.

The 37XXXD Series Vector Network Analyzer Programming Manual (10410-00262) describes all 37XXXD GPIB commands and provides programming information for operation of the VNA remotely via the IEEE-488 General Purpose Interface Bus. Included at the rear of that manual is the 37XXXD Series Vector Network Analyzer GPIB Quick Reference Guide (10410-00263).

1-7 STANDARD OPTIONS

Options that are available on the 37XXXD family are shown in the list below:

- **Option 1:** Rack Mounts with Slides
- **Option 1A:** Rack Mounts without Slides
- **Option 2A:** High Speed Time Domain
- **Option 4A:** External SCSI Disk Drive (internal hard drive removed)
- **Option 7A, 7N, 7NF, or 7S:** Replace Test Port Connectors with Type GPC-7, N, NF, or 3.5 mm
- **Option 15K:** Front Panel Access Connections for Samplers (K connectors only)
- **Option 15V:** Front Panel Access Connections for Samplers (V connectors only)

Contact your local Anritsu representative for information about installing any of the above options for the 37XXXD family.

Note

Many options that were available in 37XXXA/B/C families are now standard and installed in all models of the 37XXXD family. Examples of this are Options 3, 10, 10A, and 12.

1-8 SERVICE STRATEGY

This section provides an overview of the VNA service strategy and available service facilities. It also provides references to the information in various locations in this manual needed to accomplish the required service functions.

Functional Assembly Level Troubleshooting

The VNA modular design, extensive built-in diagnostics, and automated service tools are designed to support fast exchange of functional assembly level repairs.

Failed assemblies are not field repairable. Once an assembly is found to be faulty, it should be returned to an authorized Anritsu Service Center for exchange. Refer to the description of the Exchange Assembly Program in Chapter 2, Replaceable Parts.

The procedures for troubleshooting a failed VNA are described in Chapter 7, Troubleshooting.

Internal Hardware Adjustments and Calibrations

There are five automated internal hardware field calibrations. Two of them are used to characterize the VNA frequency and power generation sub-systems. These calibrations insure fast, consistent phase lock of system frequencies and proper compensation, leveling, and flatness of system power at the front panel test ports.

To conduct these calibrations, you need only connect the appropriate test equipment (counter or power meter) to the VNA and initiate the calibration. The VNA will control itself and the externally connected test equipment to perform measurements and store calibration constants in its internal battery backed RAM (BBRAM).

The procedures for adjusting the VNA are described in this manual in Chapter 6, Adjustments.

Internal Service Log

The VNA continuously monitors itself for proper operation. Should a failure occur, it notifies the user via a failure message on the display screen. (In remote-only operation, it also sets the GPIB Status Byte, if enabled.) It also writes the error message along with some data pertinent to the failure to an internal service log stored in battery backed memory.

The service log can be checked at any time to view (without erasing) all error messages that were written into it. It is capable of storing more than 30 pages of service messages and data. The VNA will automatically remove the oldest errors first to make room for new errors, if necessary. To check the contents of the service log, use the procedure described in Chapter 4, Operational Performance Tests.

> ***NOTE***
>
> A printed or disk file copy of the Service Log (with the failure in question) must be made available to Anritsu when exchanging a failed assembly, or when requesting service support. Refer to Chapter 2, Replaceable Parts, for further information.

System Test/Certification

Quick operational checkout of the system may be accomplished by the system user or for incoming inspection purposes using the "Operational Checkout" chapter in the 37XXXD Operation Manual. Those procedures are useful in quickly verifying that the instrument's primary measurement functions are operational and stable.

Full operational testing of the system is detailed in Chapter 4, Operational Performance Tests (or Appendix D for ME7808B/C systems). These tests should be performed annually or whenever a measurement problem is suspected.

Verification of the system's measurement accuracy and other key performance parameters may be done using the procedures in Chapter 5, System Performance Verification (or Appendix D for ME7808B/C systems). This should be performed annually or whenever a measurement problem is suspected.

Servicing Specially Modified Instruments

Instruments with customer requested special modifications performed by Anritsu will have an identifying Specials Modification number printed on the rear panel. This number will be preceded with the letters SM, that is, SM1234 is special modification number 1234. This manual contains information on servicing instruments fitted with SM5955 (67 GHz operation).

Special instruments may have service requirements different from those specified in this manual. Contact your local Service Center if you need more information when servicing such instruments.

1-9 SERVICE SUPPORT

The following sections briefly describe the various service support services and aids available to you to help you maintain your VNA.

Technical Support

Technical service support is available by contacting any Anritsu Worldwide Service Center (refer to Table 2-1), or service support may be obtained directly from the factory by contacting:

Anritsu Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

Service Software The service software listed below is contained on the diskette located at the rear of this manual:

Anritsu 37XXX Test Software (2300-178).

This software contains a series of automated tests designed to insure the VNA signal paths are functioning properly and capable of supporting stable calibrations and measurements. See the "Operational Performance Tests" chapter for details.

Anritsu 37XXX Performance Verification Software (2300-480 or 2300-496).

This software is used to verify the VNA's published measurement accuracy and traceability to the U.S. National Institute of Standards and Technology (NIST). See the "System Performance Verification" chapter for details.

> ***NOTE***
> Use of 2300-496 is required for verification of broadband systems using W1 coaxial connectors

Verification Kits

The Anritsu Verification Kits listed below are used in conjunction with the 37XXX Performance Verification Software.

N Verification Kit (Model 3663)

Contains precision N Connector components with characteristics that are traceable to the NIST.
Use for models with Option 7X connectors.

3.5 mm Verification Kit (Model 3666)

Contains precision 3.5 mm Connector components with characteristics that are traceable to the NIST.
Use for models with Option 7X connectors.

GPC-7 Verification Kit (Model 3667)

Contains precision GPC-7 Connector components with characteristics that are traceable to the NIST.
Use for models with Option 7X connectors.

K Verification Kit (Model 3668)

Contains precision K Connector components that are traceable to the NIST.

V Verification Kit (Models 3669B and Model SC7406)

Contains precision V Connector components that are traceable to the NIST. Model 3669B is for operation to 65 GHz only. Model SC7406 is for operation to 67 GHz (SM5955).

W1 Calibration/Verification Kit (Model 3656)

Contains calibration and verification W1 connector components for use with the ME7808B/C Broadband System (refer to Appendix D).

Failed Assembly Exchange Program

The exchange program allows a customer to quickly exchange a failed subassembly for a factory refurbished, fully system-tested unit that is under warranty. This results in significant time and price savings as compared with ordering a new assembly. Refer to Chapter 2, Replaceable Parts, for a complete list of exchangeable assemblies for all series 37XXXD models.

1-10 PERFORMANCE SPECIFICATIONS

The performance specifications for all Series 37XXXD models are contained in the technical data sheet located in Appendix C, Lightning 37000D Technical Data Sheet.

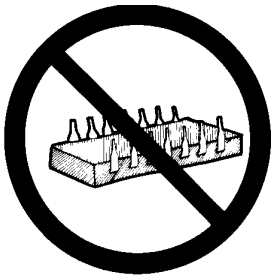
1-11 SERVICE CENTERS

Anritsu Company offers a full range of repair and calibration services at fully staffed and equipped service centers throughout the world. Table 2-1, located on page 2-2, lists all Anritsu services centers.

1-12 STATIC SENSITIVE COMPONENT HANDLING PROCEDURES

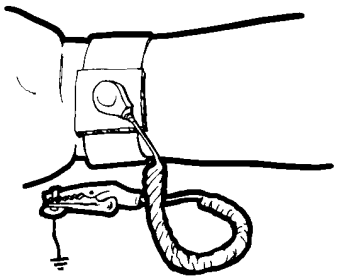
The VNA contains components that can be damaged by static electricity. Figure 1-2 illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

1. Do not touch exposed contacts on any static sensitive component.



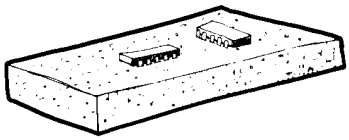
2. Do not slide static sensitive component across any surface.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

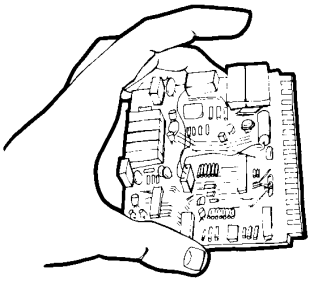


4. Wear a static-discharge wristband when working with static sensitive components.

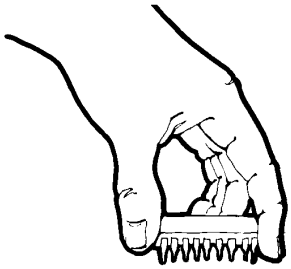
5. Label all static sensitive devices.



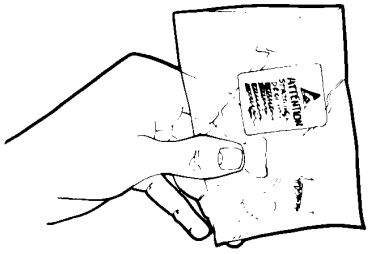
6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.



9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-2. *Static Sensitive Component Handling Procedures*

1-13 RECOMMENDED TEST EQUIPMENT

Table 1-1 lists the recommended test equipment to be used for all maintenance activities for all Series 37XXXD models. Note the "Use" codes listed in the right hand column of the table. These codes list the applicable maintenance activities for the equipment listed.

Table 1-1. *Recommended Test Equipment (1 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE**
Computer/Controller	PC with Windows 95 or later and National Instruments GPIB hardware and software.	Any	O, P
Test Software	Automates testing of VNA, Software Version 4.01 and subsequent	Anritsu 2300-178	O
Floppy Disk	Formatted, IBM PC format	DS/HD 1.44 Mbyte	A
GPIB Cable	IEEE 488-2 compliant	Anritsu 2100-2, or equivalent	O, P, A
Adapter	Anritsu K to V	Anritsu 34VFK50	A
BNC Cable	Length, 4 ft., 2 each	Any	O
Thru Line	For instruments with GPC-7 connector Test Ports: For instruments with K connector Test Ports: For instruments with V connector Test Ports:	Anritsu 3670A50-2, 3671A50-2 Anritsu 3670K50-2, 3671K50-2 Anritsu 3670V50-2	O, P
Calibration Kit	For instruments with Option 7A: For instruments with Option 7N or 7NF: For instruments with Option 7S: For instruments without Option 7: For models 37X77D, 37X97D: For instruments with SM5955:	Anritsu 3651-1* Anritsu 3653 Anritsu 3650-1* Anritsu 3652-1* Anritsu 3654B or Anritsu 3654C-1 Anritsu SC7556	O, P
Performance Verification Software	Automates performance verification testing	Anritsu 2300-496 (for ME7808B/C system only) or Anritsu 2300-480 (excludes W1 connector support) Anritsu SC7440 (for SM5955)	P
Verification Kit	For instruments with Option 7A: For instruments with Option 7N or 7NF: For instruments with Option 7S: For instruments without Option 7: For models 37X77D, 37X97D: For instruments with SM5955:	Anritsu 3667 Anritsu 3663 Anritsu 3666 Anritsu 3668 Anritsu 3669B Anritsu SC7406	P

* Calibration Kit sliding load (Option {-1}), required for Performance Verification only.

** USE CODES:
- A Adjustment / Internal Hardware Calibration
- O Operational Testing
- P Performance Verification
- T Troubleshooting

Table 1-1. *Recommended Test Equipment (2 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE**
Assurance Air Line	*None*	Anritsu model T2023-2 (K connector) or Anritsu model T2025-2 (V connector)	O
Offset Termination	37XXXD models with K Test Ports 37XXXD models with V Test Ports	Anritsu 29KF50-15 Anritsu SC4417	O
Frequency Counter	*Frequency:* 0.1 to 26.5 GHz *Input Impedance*: 50Ω	EIP Microwave, Inc., Model 578B (Must be EIP brand with Band 3 input to 26.5 GHz and GPIB interface) or Anritsu MF2413B	A, O O
Digital Multimeter	*None*	Any	T
Oscilloscope	*None*	Tektronix, Inc. Model 2445	T
Power Meter 1, with: Power Sensor 1 ***or:*** Power Meter 2, with: Power Sensor 2	*Power Range:* –30 to +20 dBm (1 mW to 100 mW) *Other:* GPIB controllable *Frequency Range:* Useable to the full frequency range of the VNA *Power Range:* –70 to +47 dBm (100 pW to 50 W) *Other:* GPIB controllable *Frequency Range:* 0.01 to 40 GHz	Anritsu Model ML243xA Power Meter MA2474A (40 GHz and below) Model SC6230 (to 65 GHz) Gigatronics 8541 or 8542 Gigatronics 80304A	A, O A, O

** USE CODES:
- A Adjustment / Internal Hardware Calibration
- O Operational Testing
- P Performance Verification
- T Troubleshooting

Chapter 2
Replaceable Parts

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Anritsu Customer Service Centers

UNITED STATES

Anritsu Company
490 Jarvis Drive
Morgan Hill, CA 95037-2809
USA
Telephone: 1-800-Anritsu
FAX: 408-776-1744

Anritsu Company
10 New Maple Ave., Unit 305
Pine Brook, NJ 07058
USA
Telephone: 1-800-Anritsu
FAX: 201-575-0092

Anritsu Company
1155 E. Collins Blvd
Richardson, TX 75081
USA
Telephone: 1-800-Anritsu
FAX: 972-671-1877

AUSTRALIA

Anritsu Pty. Ltd.
Unit 21/270 Ferntree Gully Road
Notting Hill, Victoria 3168
Australia
Telephone: 03-9558-8177
FAX: 03-9558-8255

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Anritsu Eletrônica Ltda.
Praça Amadeu Amaral 27, 1º andar.
Bela Vista, São Paulo, SP, Brasil.
CEP: 01327-010
Telephone: 55-11-3283-2511
Fax: 55-11-3288-6940

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Anritsu Instruments Ltd.
700 Silver Seven Road, Suite 120
Kanata, Ontario K2V 1C3
Telephone: (613) 591-2003
FAX: (613) 591-1006

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(Shanghai) Company Ltd.
2F, Room B,
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No 516 Fu Te Road (N)
WaiGaoQiao Free Trade Zone
Pudong, Shanghai 200131, P.R.
China
Telephone: 21-5868-0226
FAX: 21-5868-0588

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Anritsu S.A.
16/18 Avenue du Quebec
SILIC 720
91961 Courtaboeuf Cedex
Telephone: 016-09-21-550
FAX: 016-44-61-065

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Anritsu GmbH
Konrad-Zuse-Platz 1
Muenchen 81829
Germany
Telephone: 089-442308-0
FAX: 089-442308-55

INDIA

Meera Agencies (P) Ltd.
23 Community Centre
Zamroodpur
Kailash Colony Extension
New Delhi, 110 048
Telephone: 91-11-6442700
FAX: 91-11-6442500

ISRAEL

Tech-Cent, Ltd.
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Tel-Aviv 69719
Telephone: 03-64-78-563
FAX: 03-64-78-334

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Anritsu S.p.A
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00144 Roma EUR
Telephone: 06-50-99-711
FAX: 06-50-22-4252

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Telephone: 02-553-6603
FAX: 02-553-6605

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Anritsu Customer Service Ltd.
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FAX: 046-225-8379

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Singapore 118502
Tel: 6-282-2400
FAX: 6-282-2533

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ETECSA
12 Surrey Square Office Park
330 Surrey Avenue
Ferndale, Randburg, 2194
South Africa
Telephone: 27-11-787-7200
FAX: 27-11-787-0446

SWEDEN

Anritsu AB
Borgafjordsgatan 13
164 40 Kista Sweden
Telephone: 46-8-53470700
FAX: 46-8-53470730

TAIWAN

Anritsu Co., Inc.
7F, No. 316, Section 1
Nei Hu Road
Taipei, Taiwan, R.O.C.
Telephone: 02-8751-1816
Service Telephone: 02-8751-2126
FAX: 02-8751-1817

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200 Capability Green
Luton, Bedfordshire
LU1 3LU, England
Telephone: 015-82-43-3200
FAX: 015-82-73-1303

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http://www.us.Anritsu.com/contacts/default.aspx?lc=Eng&cc=US&rc=ARO

and choose a country for regional contact information.

Anritsu Part Number: 00986-00211, updated July 31, 2007

Chapter 2
Replaceable Parts

2-1 INTRODUCTION

This chapter provides replaceable parts information for all 37XXXD models. The major replaceable VNA assemblies and parts are listed and locations shown in this chapter. Parts and assemblies that are found on on the ME7808B/C Broadband systems are itemized in Appendix D.

2-2 EXCHANGE ASSEMBLY PROGRAM

Anritsu maintains a module exchange program for selected subassemblies. If a malfunction occurs in one of these subassemblies, the defective item can be exchanged. Upon receiving your request, Anritsu will ship the exchange subassembly to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies or RF assemblies are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

> ***NOTE***
>
> When sending a failed assembly to the factory for exchange, a copy of the Service Log *must always* accompany the failed assembly. This copy may be a printout, or a saved disk copy. Due to the importance of the service log information to the Anritsu factory Service Engineers, the exchange prices are only valid if the service log data is included with the failed assembly.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative (Table 2-1) or call Anritsu Customer Service direct (refer to Section 2-4.

2-3 REPLACEABLE SUBASSEMBLIES AND PARTS

All items shown in Tables 2-2 and 2-3 are exchange items. All items shown on Table 2-4 are non-exchange items except for the power supply, which is an exchange item.

2-4 PARTS ORDERING INFORMATION

All parts listed in Tables 2-2 through 2- 4 may be ordered from your local Anritsu service center (Table 2-1, page 2-2). Or, they may be ordered directly from the factory at the following address:

Anritsu Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

Table 2-2. *Printed Circuit Board Assemblies*

Reference Designator	Assembly / Part	Original Part Number	Replacement Part Number
A1	First Local Oscillator	57661-3	ND60314
A2	Second Local Oscillator	61835-3	61835-3
A3/A6	Test A, Test B IF Processor	D38503-3	D38503-3
A4	Reference IF Processor	D41794-5	D41794-5
A5	Analog to Digital Converter	D38505-4	D38505-4
A7	10 MHz/LO3	61181-3	ND62436
A8	Source Lock/ Separation Control	60866-3	ND60702
A9	Main Processor	62414	ND63005
A13	Floppy Drive Control I/O #1	D38513-4	D38513-4
A14	I/O #2	D38514-3	D38514-3
A15	Graphics Processor	D42281-3	D44281-3
A16	Hard Disk	D41041-5	ND62315
A18	Rear Panel PCB	61011-3	61011-3
A19	Front Panel Switch PCB	D44279-3	D44279-3
A20	Front Panel Switch Control	D44280-3	D44280-3
A21A1	Signal Source YIG/Bias Control	48512-3	48512-3
A21A2	Signal Source Control/ALC	61184-3	61184-3
A24	VME Bus Terminator	D38524-3	D38424-3
A26	Ext. Keybd Static Protection	58534-3	58534-3

NOTE
The VNA A17 Motherboard PCB Assembly is not a field-replaceable item.

Table 2-3. *RF Source and Test Set Assembly RF/Microwave Components*

Assembly / Part Description	Original Part Number	Replacement Part Number
YIG Oscillator (all models)	C21620-1	C21620-1
Switched Filter (all models)	D45244	D45244
Source Down Conversion Module (all models)	D27532	D27532
Coupler (20 and 40 GHz models)	D29422	D29422
Coupler (50 and 65 GHz models)	ND52929	ND52929
Source Doubler Module (all models)	47520	47520
Transfer Switch (20 and 40 GHz models)	46535	46535
Transfer Switch (50 and 65 GHz models)	D27030-2	D27030-2
Step Attenuator (20 and 40 GHz models)	4612K	4612K
Step Attenuator (50 and 65 GHz models)	ND52564	ND52564
Bias Tee (20 and 40 GHz models)	48383	48483
Bias Tee (50 and 65 GHz models)	53409	53409
Sampler/Down Conversion Module (all models)*	58437	ND61660
Power Amplifier (all models)*	56650	ND61660
SPDT Switch (50 and 65 GHz models)	29855	29855
Source Quadrupler Module (50 and 65 GHz models)	60129	60129
MUX Coupler (Port 1 side, 50 and 65 GHz models)	49470-1	49470-1
MUX Coupler (Port 2 side, 50 and 65 GHz models)	49480-1	49480-1
Shaped Pad (50 and 65 GHz models)	52956**	52956**
3 dB Fixed Attenuator, V Connectors	ND26178	ND26178
37 GHz Hi-Pass Filter (50 and 65 GHz models)	49247	49247
16.8 GHz Lo-Pass Filter (50 and 65 GHz models)	B28612	B28612

* The Sampler/Down Conversion Module and Power Amplifier must be replaced as a single assembly.
** For instrument serial numbers 051600 or above, use part number: 64350

Table 2-4. *Miscellaneous Replaceable Subassemblies and Parts**

Assembly / Part Description	Replacement Part Number
Floppy Disk Drive	2000-1364
Fan	ND54935
Power Supply	ND63006
LCD display	15-100
Backlight Driver PCB for LCD	2000-1365
Basic Measurement Software (“BMS”, 2 disk set)	2300-500
Backup battery for A9 PCB	Purchase Locally
Boot Firmware for A9 PCB	58-1321
Cable, front panel for Opt.15 (20 and 40 GHz models)	B18265-201
Cable, front panel for Opt.15 (50 and 65 GHz models)	B35569-195

* All items on this Table are non-exchange items except for the power supply.

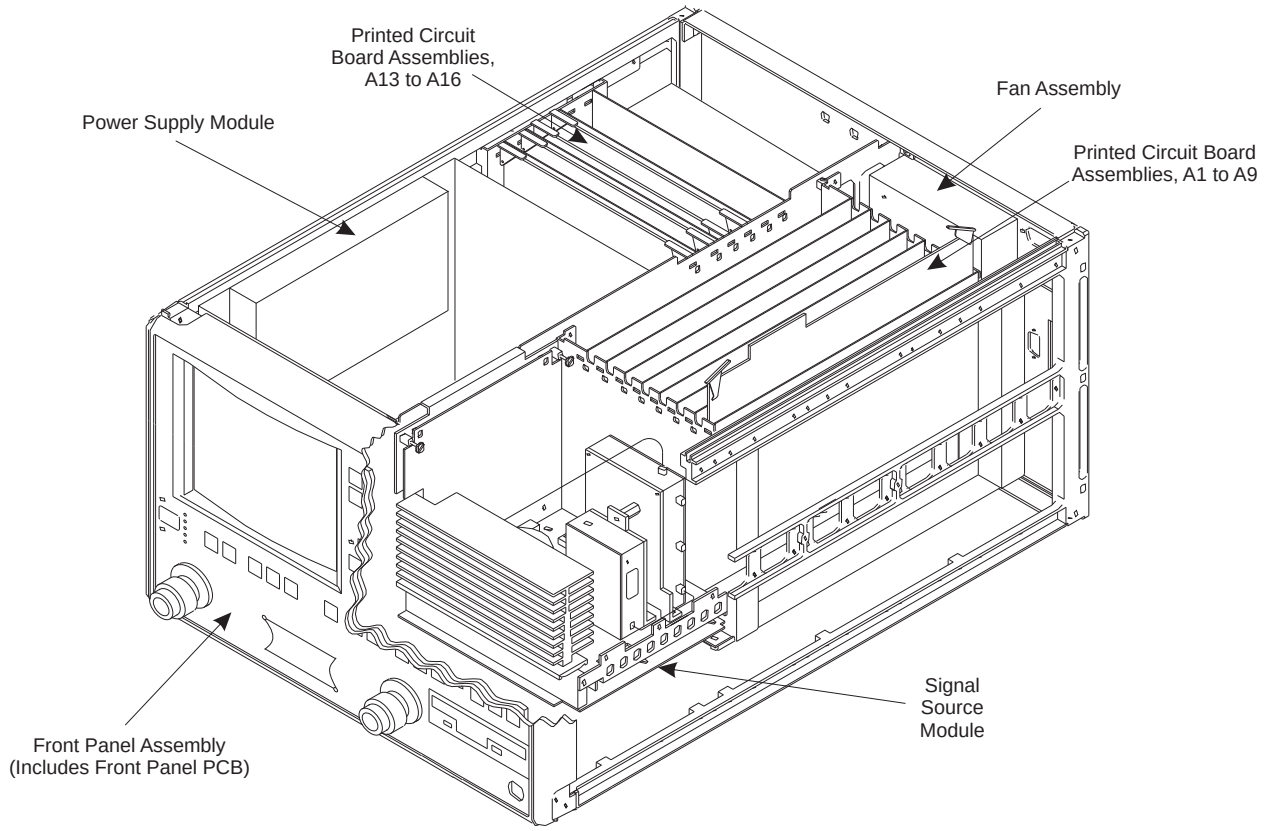


Figure 2-1. *Major Assemblies Location Diagram (Top View)*

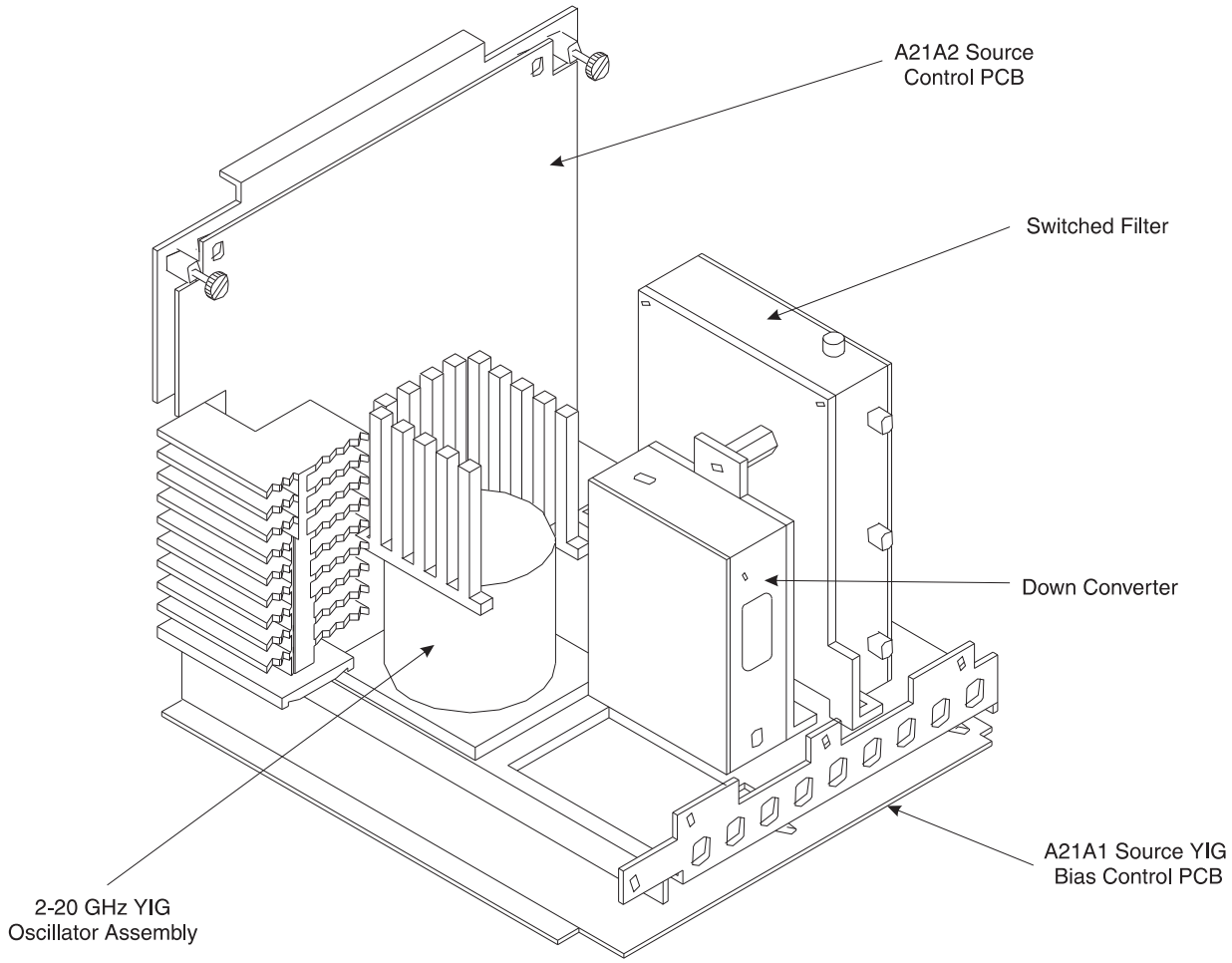


Figure 2-2. *Signal Source Parts Location Diagram*

Chapter 3
Theory of Operation

Table of Contents

Chapter 3
Theory of Operation

3-1 INTRODUCTION

This chapter provides a brief overview of the functional assemblies and major parts that comprise a typical 37XXXD VNA system. It also briefly describes the operation of each major assembly. Further details of the ME7808B/C Broadband system are found in Appendix D.

3-2 SYSTEM OVERVIEW

37XXXD Vector Network Analyzers are ratio measurement systems used to measure complex vector signal characteristics (real/imaginary, magnitude/phase, etc) of devices and systems in the 40 MHz to 65 GHz frequency range.

The VNA performs these measurements by sourcing a stimulus signal to the Device Under Test (DUT) that is connected to the front panel Port 1 and/or Port2 connectors. (See Figure 3-1 or 3-2). It simultaneously measures the DUT response, which consists of reflected and/or transmitted (attenuated, or amplified) signals at the connectors of the DUT. The reflected and/or transmitted signal(s), and a sample of the stimulus signal, are down converted and then transformed into their real and imaginary vector components. The resultant vector components are measured and converted into digital information. This digital information is sent to the Main Processor PCB where the desired S-parameter data is normalized and then presented to the user via the front panel color display. The display information is also sent to the rear panel VGA Out connector for use with an external VGA monitor.

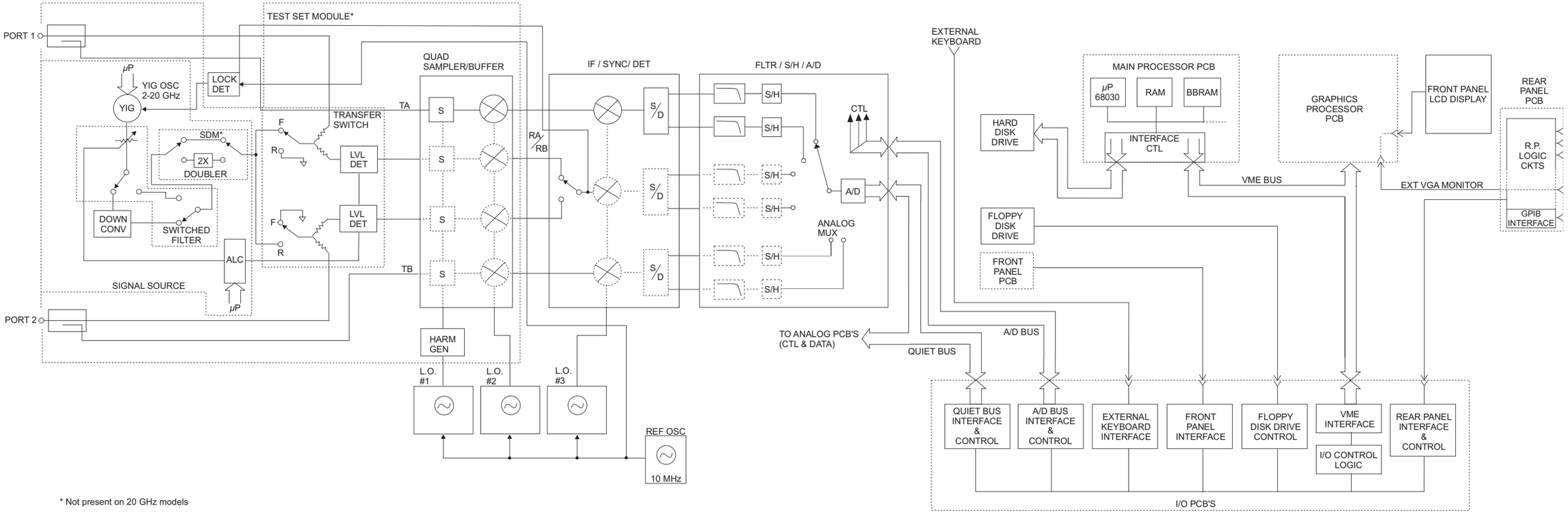
The normalized measurement information is also sent to the rear panel Printer Out connector for use with an external printer and/or plotter.

A front panel keypad, a rotary knob, and an IBM compatible keyboard interface provide user interaction with VNA Main Processor PCB.

The system is equipped with internal hard disk and floppy disk drives and battery backed internal memories for storage and retrieval of data and front panel setup information.

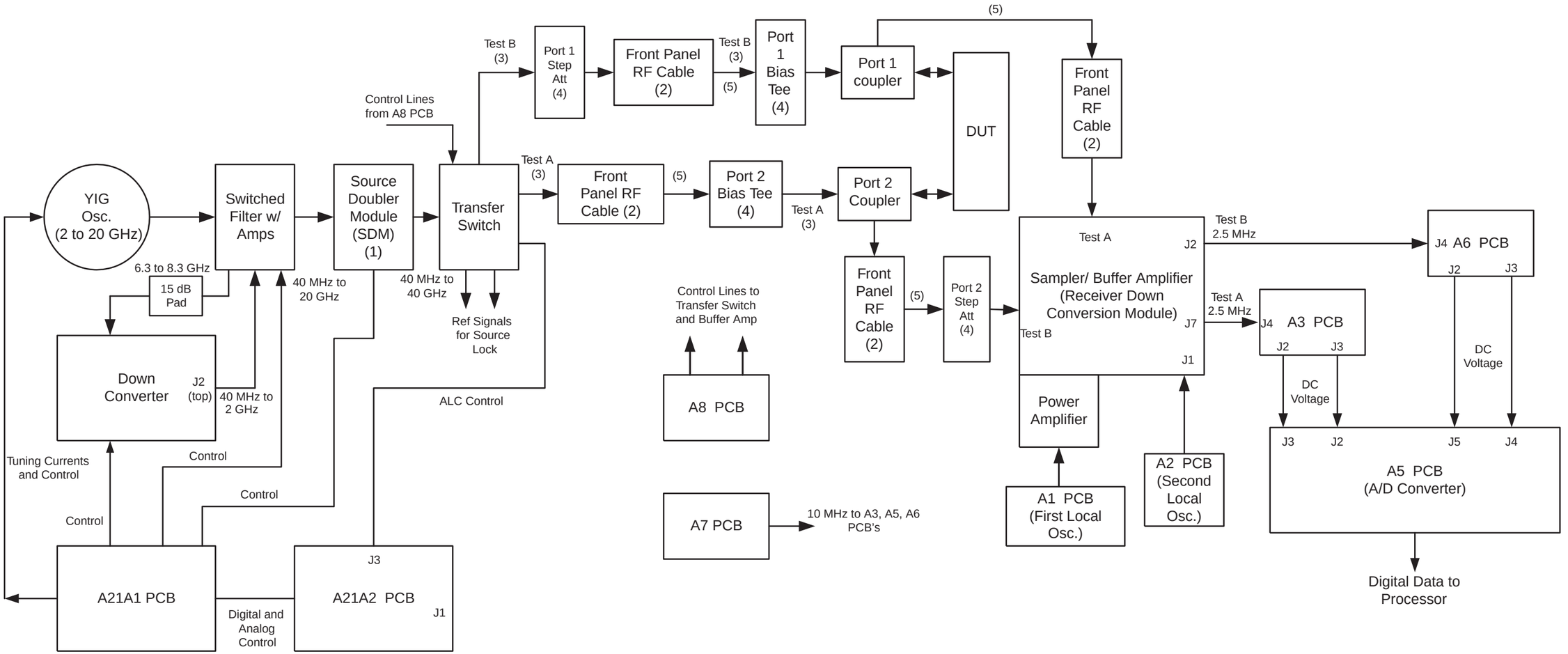
The VNA implements an IEEE 488.2 interface. This GPIB interface allows an externally connected instrument controller to control the VNA system in the “Remote-Only” mode. All VNA measurement and input/output operations may be controlled remotely in this mode.

An internal service log stores a record of system failures, data about the failures, and other key system service information. The service log is implemented using internal battery-backed SRAM memory.



* Not present on 20 GHz models

Figure 3-1. *Overall Block Diagram of RF Source, Typical Test Set and Receiver Down Conversion Modules*



Notes:

(1) Not present on 20 GHz models.

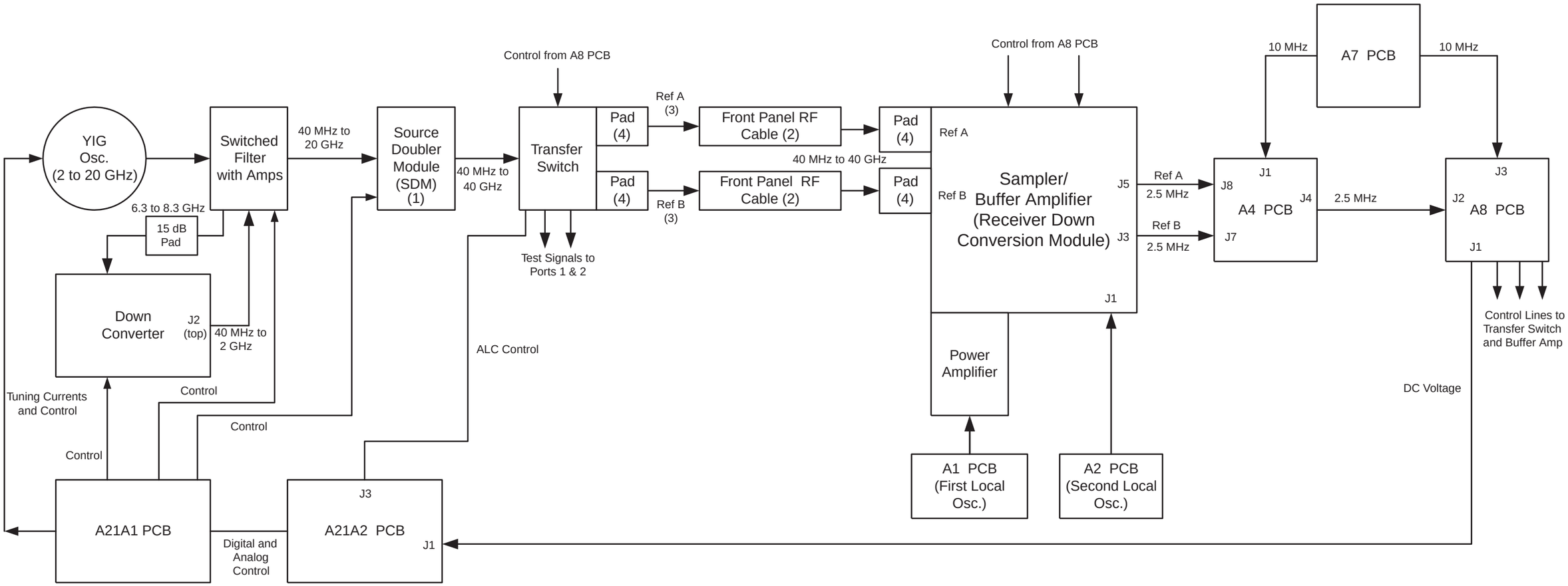
(2) Option 15 units only.

(3) When using S21, S12 or Non-Ratio (diagnostics) displays. Test A = b1, Test B = b2.

(4) Not present on 372XXD models.

(5) Fixed attenuator may be present . Value will vary with model.

Figure 3-2. *Test Signal Paths for 20 GHz and 40 GHz Models*



Notes:

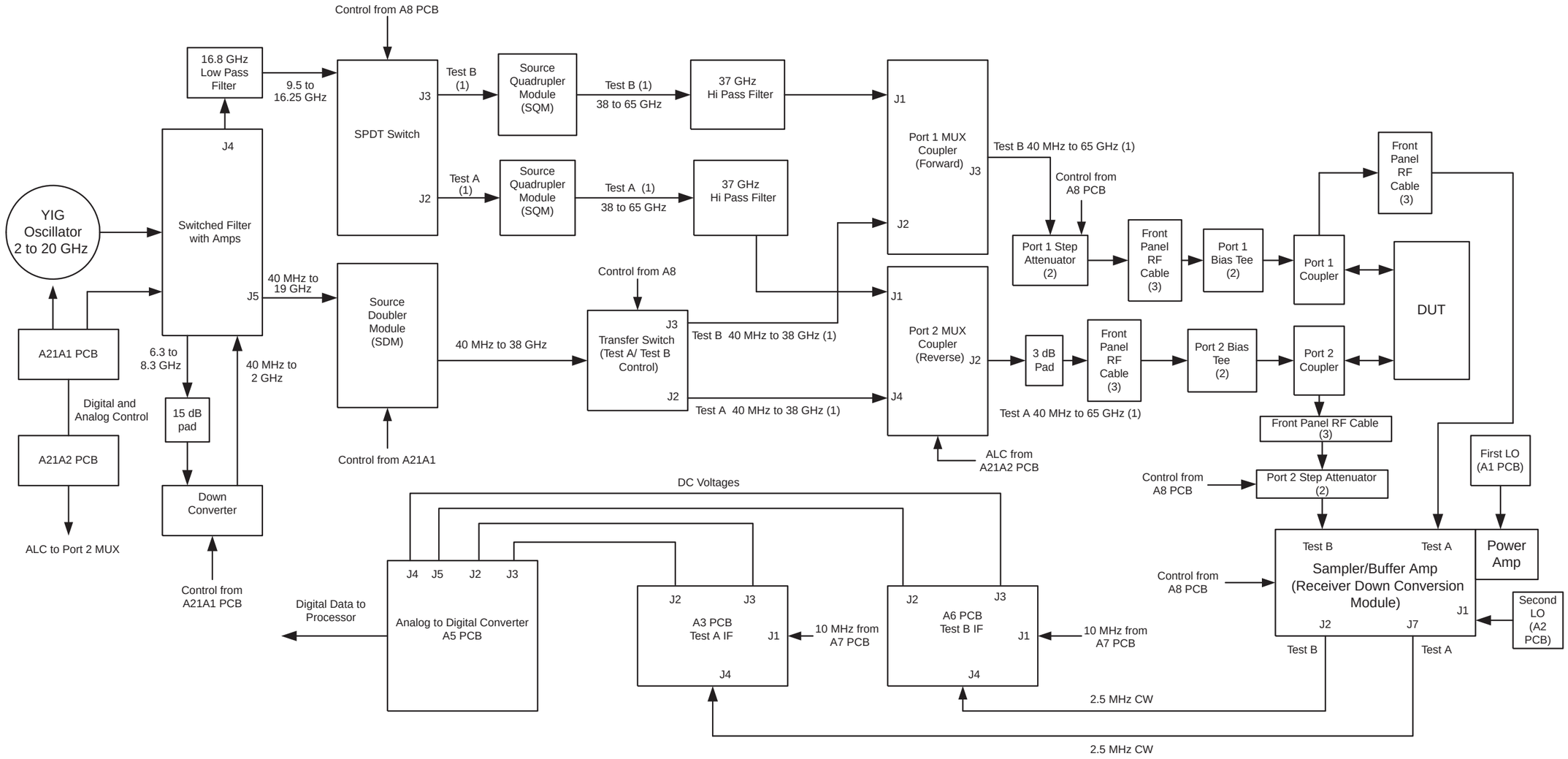
(1) Not present on 20 GHz models.

(2) Option 15 units only.

(3) Ref A = a1, Ref B = a2.

(4) Fixed attenuator may be present. Value will vary with model.

Figure 3-3. *Source Lock Signal Paths for 20 GHz and 40 GHz Models*



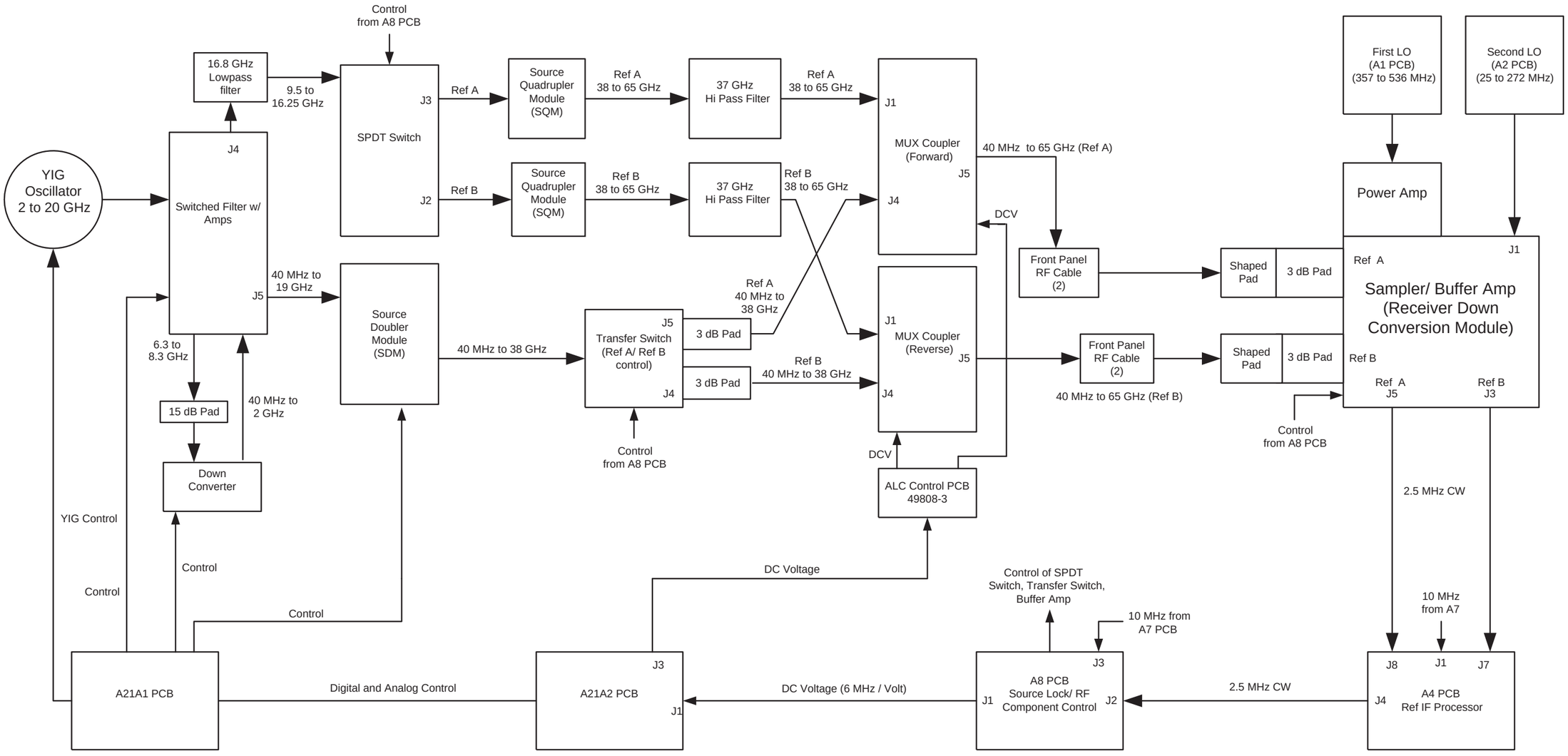
Notes:

(1) When using S21, S12, or Non-Ratio (diagnostic) displays. Test A = b1, Test B = b2.

(2) Not present on 372XXD models.

(3) Option 15 units only.

Figure 3-4. *Test Signal Paths for 50 GHz and 65 GHz Models*



Notes:
(1) Ref A = a1, Ref B = a2.
(2) Option 15 units only.

Figure 3-5. *Source Lock Signal Paths for 50 GHz and 65 GHz Models*

3-3 ANALOG SUBSYSTEM ASSEMBLIES

The following sections briefly describe the major assemblies that comprise the VNA Analog Subsystem. Descriptions of the functions performed by each assembly are also included.

Signal Source Module

The Signal Source Module consists of the items listed below; refer to the block diagram of the Analog Subsystem (Figure 3-3).

- 2-20 GHz YIG Oscillator Assembly
- A21A1 YIG/Bias Controller PCB
- A21A2 Source Control PCB
- Switched Filter Assembly
- Down Converter Assembly

The Signal Source Module is a swept frequency signal generator that produces a phase locked (and leveled) output signal within a range of 40 MHz to 20 GHz. All 37XXXD models employ phase-lock control of the signal source module so that the output frequency is accurate and stable. The output signal is phase locked by the –6 MHz/volt control signal fed back from the A8 Source Lock/Separation Control PCB Assembly (which is described in following sections).

All Series 37XXXD VNA models use a single YIG-tuned oscillator to produce fundamental frequency source signals from 2.0 to 20 GHz. All other output frequencies are derived from the fundamental frequencies generated by the YIG-tuned oscillator. The signal source output frequencies for the low end portion of the frequency range (40 MHz to 2.0 GHz) are produced by down converting YIG fundamental signals in the range of 6.3225 to 8.3 GHz.

For 40 GHz models, the signal source output frequencies for the high end portion of the frequency range (20 to 40 GHz) are produced by the Switched Doubler Module that doubles the YIG fundamental signals in the range of 10 to 20 GHz. The Switched Doubler Module (SDM) is located in the Test Set Module (described below.) The A21A2 Source Control PCB assembly provides all bias and control signals for the SDM. 50 and 65 GHz models use an SDM to create frequencies from 20 to 38 GHz, and they use Source Quadrupler Modules (SQM's) to create frequencies above 38 GHz.

The YIG-tuned oscillator generates a high-power RF output signal that has low broadband noise and low spurious content. The frequency of the YIG-tuned oscillator is controlled by means of :

- The YIG main tuning coil
- The YIG FM (fine tuning) coil

The system A9 Main Microprocessor PCB sends the data that represents the desired operating frequency to the A21A2 (Source Control) PCB, which converts the frequency data to analog signals. These signals are then sent to the A21A1 YIG/Bias Controller PCB. This PCB converts the analog signals to YIG main tuning coil current.

The main tuning coil current from A21A1 YIG/Bias Controller PCB coarsely tunes the YIG-tuned Oscillator to within a few megahertz of the final output frequency. The YIG phase-lock loop then fine tunes the YIG-tuned oscillator to the exact output frequency via the FM (fine tuning) coil.

The RF power is controlled by the Automatic Leveling Control (ALC) circuits that are located on the A21A2 Source Control PCB. The input to the ALC circuits is the DC feed-back signal from the leveling detectors located on the Transfer Switch (20 and 40 GHz models) or the MUX couplers (50 and 65 GHz models).

Depending on the frequency of operation, the fundamental signal is passed through one of four low-pass filters located in the Switched Filter Assembly. The cut-off frequencies for these filters are 3.3 GHz, 5.5 GHz, 8.4 GHz, and 13.5 GHz, respectively. The switched filter also amplifies the RF signal by 8 to 16 dB, depending on frequency. The signal is then passed through a 20 GHz high pass filter before being routed either directly to the Test Set Module, or to the Down-Converter Assembly.

The signal is switched to the Down-Converter Assembly only when the VNA is operating in the low end portion of its frequency range. The frequency of the output signal from the Source Down Converter Assembly is 40 MHz to 2 GHz. The output signal from the Down Converter Assembly is routed to the Test Set Module.

Test Set Module, 20 GHz and 40 GHz Instruments

The major blocks that comprise the test set module for the 20 GHz and 40 GHz models are:

- Transfer Switch with ALC circuits
- Step Attenuators (not found on 200 series models)
- Bias Tees (not found on 200 Series models)
- Couplers
- Sampler/Down Coversion Module (labeled as “Sampler/Buffer/Amp”)
- Power Amp Assembly
- Source Doubler Module (not found on 20 GHz models)

Refer to Figures 3-2 and 3-3 for a graphical representation of 20 GHz and 40 GHz models and to Figures 3-4 and 3-5 for 50 GHz and 65 GHz models.

In 20 GHz models, RF from the Source Module is routed to the Transfer Switch.

In 40 GHz models, RF from the Source Module is routed into the Source Doubler Module (SDM) and, if the instrument sweep is set to any frequency above 20.0 GHz, the frequency is doubled. While the frequency of the instrument operation is below 20.0 GHz, the SDM is in a pass-through mode and no doubling occurs. The RF from the SDM output is then routed to the Transfer Switch.

RF Output from the transfer switch is simultaneously routed through two outputs in normal S Parameter operation. In this operation mode, one Reference Signal and one Test Signal is generated. The Reference Signal is critical for the phase locking of the RF Source and is used in the measurement of phase angles. The Test Signal is eventually routed to the Device Under Test and is not related to phase locking of the RF Source.

S Parameter measurements are defined as ratios of the Test to the Reference Signals and are defined as:

- S11 = Test A/Ref A = b1/a1
- S21 = Test B/Ref A = b2/a1
- S12 = Test A/Ref B = b1/a2
- S22 = Test B/Ref B = b2/a2

The full RF path of the Reference Signals is shown in Figure 3-3, Source Lock Signal Paths. The full RF path of the Test Signals in a transmission measurement (S21 or S12) is shown in Figure 3-2. In a reflection measurement (S11 or S22), Test Signals originate from the Transfer Switch opposite from what is shown in Figure 3-2. (In other words, Test A routes through the RF components on its way to Test Port 1 and Test B routes through the RF components on its way to Test Port 2).

Leveling of the RF is accomplished by detectors in the Transfer Switch that sense the levels of the Reference Signal. This detected signal is sent to the A21A2 PCB in the Source Module.

Test Signals that are routed to the DUT for test have passed through the non-coupled arm of the coupler. Signals that have passed through the DUT (or have reflected back from the DUT) are passed through the coupled arm of the couplers at the test ports. The signal received from the DUT is returned to the Sampler/Down Conversion Module (via the step attenuator for 300 series instruments).

Both Reference signals and both Test Signals are routed into the Sampler/Down Conversion Modules for down conversion to 2.5 MHz (3rd IF signal). This down conversion is accomplished by using LO1 and LO2 found on the A1 and A2 PCBs. Before use by the Sampler/Down Conversion Module, the signal from LO1 is amplified by the Power Amplifier assembly (mounted on the Sampler/Down Conversion Module) for a power gain of about 30 dB. (The Power Amplifier and Sampler/Down Conversion Module are tuned to match each other and are not replaceable separately).

The individual Test and Reference 2.5 MHz signals are routed off the Test Set Module to the A3, A4, and A6 IF Processor PCBs as shown in Figures 3-2 and 3-3.

Test Set Module, 50 GHz and 65 GHz Instruments

Refer to Figures 3-4 and 3-5 for a graphical representation of the following description:

Many RF components found in the 50 GHz and 65 GHz models perform nearly identical functions as components in the 20 GHz and 40 GHz models, with the following exceptions:

- Transfer Switch
- SPDT Switch
- Port 1 MUX Coupler
- Port 2 MUX Coupler
- Port 1 and Port 2 Source Quadrupler Modules
- 37 GHz High Pass Filters

As in the 20 GHz and 40 GHz models, two Reference Signals and two Test Signals are created. The Reference Signals are used for phase locking of the RF Source and for phase measurements. The Test Signals are routed to the DUT and are not involved in phase locking of the Source Module. One Reference Signal and one Test Signal is generated at any given time during a normal S Parameter measurement.

The formulas for the S Parameters are the same as described above. After the signals are received from the DUT, the down conversion scheme is identical to the 20 GHz and 40 GHz models (described above).

The RF from the Source Module is routed to either the SPDT switch or to the SDM. Signals routed to the SPDT switch will eventually become signals used by the instrument while operating over 38 GHz, and signals routed to the SDM will be used by the instrument while operating below 38 GHz.

When operating below 38 GHz, signals pass through the SDM (through the pass-through or doubling sections) and are routed to the Transfer Switch (a different model switch than is used in the 20 GHz and 40 GHz instruments). The signal path and down conversion scheme is nearly identical to the 20 GHz and 40 GHz instruments, with the exception of the Port 1 and Port 2 MUX coupler circuits, which are used to pass above-38 GHz or below-38 GHz signals at the appropriate time during the sweep. ALC control is accomplished using the Port 1 and Port 2 MUX couplers.

When operating above 38 GHz, the signal from the 16.8 GHz lowpass filter of the Source Module is fed into a simple SPDT switch. If the instrument is sweeping in the forward mode (S21 or S11), RF is then switched into the Port 1 (Ref A) Source Quadrupler Module (SQM). If in the reverse mode (S12 or S22), RF is switched into the Port 2 (Ref B) SQM. Signals then pass through the 37 GHz High Pass Filters and Test Signals are created within the Port 1 and Port 2 MUX couplers.

Reference Signal paths remain as shown in Figure 3-3 for all four S Parameters. Test Signal paths for transmission measurements are as shown in Figure 3-4, but during reflection measurements, Test A and Test B Signal paths are swapped (Test A is emitted from Port 1 during S11, and Test B is emitted from Port 2 during S22 measurements).

A7 PCB 10 MHz Timebase

The 10 MHz system clock is based on an OCXO mounted on the A7 PCB. The A7 PCB also contains a fixed 2.42 MHz Local Oscillator and an 80 kHz calibration signal. The 80 kHz calibration signal is periodically sent to the A3, A4, and A6 PCBs for self-calibration of IF amplifier circuits. (This occurs during the time when the message, “Calibrating IF, please wait” is displayed on the VNA.)

Receiver Module

The Receiver Module consists of the items listed below (refer to Figure 3-3):

- Quad Sampler/Down Conversion Module with integrated SRD (step recovery diode)
- Power Amplifier
- A1, LO1 PCB
- A2, LO2 PCB

The Receiver Module is based on a four channel, two stage Sampler/Down Conversion module that converts the 40 MHz to 65 GHz signals to 2.5 MHz signals.

The first stage of the Receiver Module uses harmonic sampling to down-convert the four 40 MHz to 65 GHz output signals from the Test Set Module down to 89 MHz signals. Any input signals below 270 MHz are passed directly through the four harmonic samplers to the second stage without down-conversion. The drive signal to each of the harmonic samplers is a comb of harmonics generated by a step recovery diode (SRD).

The Power Amplifier provides the signal that drives the SRD. The input to the Power Amplifier is the 357 to 536.5 MHz signal from the A1 First Local Oscillator (LO1) PCB. Regardless of the operating frequency, the Power Amplifier is biased on at all times to insure optimum thermal stability.

The second stage of the Receiver Module uses the 25.0 to 272.5 MHz signal from the A2 Second Local Oscillator (LO2) PCB to down-convert the 89 MHz signals into four 2.5 MHz IF signals TA, TB, RA, RB (two test signals and two reference signals). Either the Reference A or the Reference B IF signal is selected, as is appropriate for Forward/Reverse operation. The resultant three 2.5 MHz IF signals (Test A, Test B, and Reference A/B) are output to the IF Section. A buffered version of the Reference A/B signal is also fed to the A8 Source Lock/Signal Separation Control PCB as the Source Lock signal.

The Receiver Module can also select the Reference A IF signal that is output to the IF Section via the Test A switch path. This IF signal is used during Line Reflect Line (LRL) Calibrations to ratio the Reference A and Reference B signals.

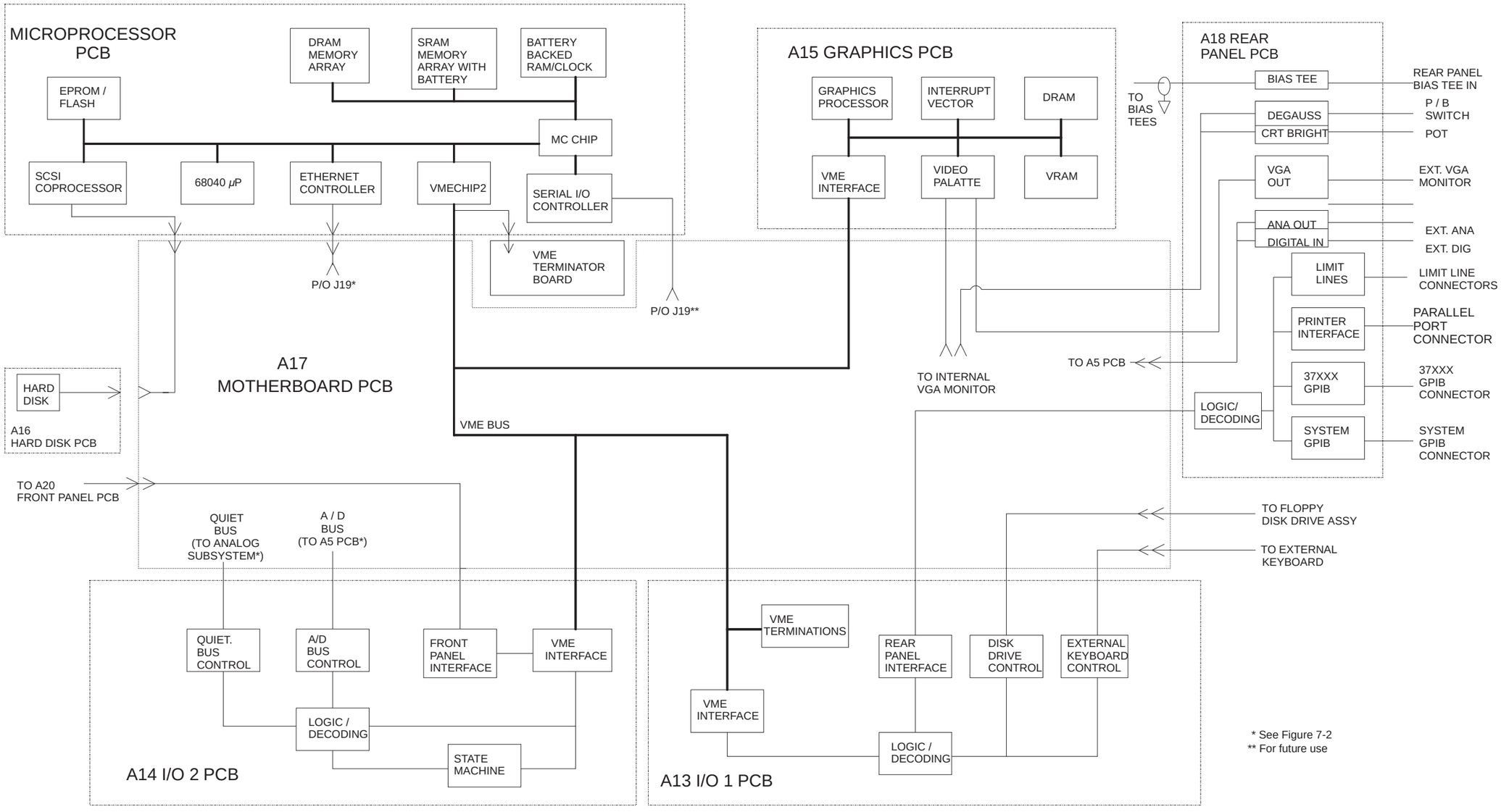


Figure 3-6. *DigitalSubsystem Block Diagram*

A8, Source Lock/Signal Separation and Control PCB

The Source Lock Phase Comparator circuit on the A8 Source Lock/ Signal Separation Control PCB compares the Source Lock (Reference A/B) signal from the Receiver Module with a signal derived from the 10 MHz reference oscillator. The output of this circuit is the –6 MHz/V correction signal, which is routed to the circuit on the A21A2 Source Control PCB that generates the FM coil tuning current signal. This signal is output to the A21A1 YIG/Bias Controller PCB to fine tune the YIG-tuned oscillator to the exact output frequency. When the YIG-tuned oscillator outputs the exact frequency, the two inputs to the phase comparator circuit on the A8 PCB match and the phase-lock loop is locked.

The A8 PCB Assembly also provides bias and control signals to the Test Set and Receiver Modules for operating the following circuits:

- Transfer Switch
- Power Amplifier
- Quad/Down Conversion Module
- Front Panel Forward/Reverse LEDs
- Step Attenuators
- Control Signals to Model 3738A Test Set (Broadband Millimeter Wave Systems)

IF Section

The IF Section consists of the items listed below (refer to Figure 3-2):

- A3 Test A IF PCB
- A4, Reference IF PCB
- A5, A/D Converter PCB
- A6, Test B IF PCB
- A7, Third Local Oscillator, LO3, PCB

The IF Section converts the three 2.5 MHz IF signals from the Receiver Module into six DC output signals. The A3 (Test A), A4 (Reference A/B), and A6 (Test B) PCBs down-convert the 2.5 MHz input IF signals to 80 kHz IF signals and then adjust their amplitude for input to the synchronous detector stage of each PCB. Each 80 kHz IF signal is synchronously detected and converted into a pair of DC signals that contain the information for the real and imaginary portions of the original 80 kHz IF signal. Thus, the three IF signals (two test signals and the reference signal) yield six DC signals that fully represent the real and imaginary vector components of the DUT's S-parameters.

The IF Section also checks the 2.5 MHz phase lock signal for proper power level by comparing it to a known reference level on the A4 PCB. A sample of the 2.5 MHz Reference A/B IF signal is sent to the A8 Source Lock/Separation Control PCB assembly for phase locking the signal source module. The A3 and A6 PCBs are functionally identical and physically interchangeable.

A7 PCB, LO3 The A7, Third Local Oscillator (LO3) Assembly, provides a fixed 10 MHz Reference Timebase and a 2.42 MHz Local Oscillator signal that is used on the A3, A4, and A6 PCBs to down-convert the 2.5 MHz IF signals to 80 kHz. It also provides an 80 kHz standard signal for the IF Section Calibration process that occurs automatically approximately every six minutes. This automatic IF Section Calibration is one of the VNA features that ensures rated measurement accuracy. Automatic IF Calibration can be turned off and/or invoked at any time during measurement sweeps.

A5 A/D Converter PCB The A5 A/D Converter PCB contains a six-channel, two stage, switched-filter sample-and-hold circuit and a 20 bit A/D converter. Each of the six DC signals from the A3, A4, and A6 PCBs are input to a separate channel of the PCB. The first stage of each channel is a low-pass filter with four selectable cutoff frequencies of 10 kHz, 1 kHz, 100 Hz, and 10 Hz. The second stage of each channel is a sample-and-hold amplifier that stores the signals during the A/D conversion process. Each channel is sequentially selected for input to the 20 bit A/D converter.

The A5 A/D Converter PCB also derives the 109.89 kHz Power Supply Synchronization Signal and the 80 kHz IF Synchronization Signal from the 10 MHz Reference Timebase. Additional functions of the A5, A/D Converter Assembly include:

- Measurement of power supply voltages and other internal nodes of the 37XXXD for diagnostic purposes.
- Measurement of an externally applied analog input signal. This function is used for service purposes only.
- External Trigger Input signal processing (from rear panel)
- External Analog Output signal generation (to rear panel)

The A/D converter circuitry located on the A/5 PCB is used as a DVM to measure various internal system analog monitor points on the A1 to A8 and A21A1/ A21A2 PCBs. It is also used to monitor power supply voltages and other critical points throughout the VNA, which can be readout via the Diagnostics Menus. DVM readings are also recorded in the service log for certain system failures.

> ***NOTE***
> If this PCB is replaced, switch settings on the new PCB must be changed to match settings of the old PCB.

3-4 DIGITAL SUBSYSTEM ASSEMBLIES

The following sections briefly describe the major assemblies that comprise the VNA Digital Subsystem. The digital subsystem provides all system control, I/O interface, digital signal processing, and data presentation functions. The major assemblies that comprise the VNA digital PCB subsystem are listed below (refer to Figure 3-4):

- A9, Main Processor PCB
- A13, I/O Interface #1 PCB
- A14, I/O Interface #2 PCB
- A15, Graphics Processor PCB
- A16, Hard Disk PCB
- A18, Rear Panel Interface
- Rear Panel Assembly
- Front Panel Assembly
- Floppy Disk Assembly
- A24, VME Bus Terminator PCB

A9 Main Processor PCB Assembly

The major components that comprise the A9 Main Processor PCB are:

- 68040 Microprocessor (w/ integrated co-processor)—This is the CPU for the 37XXXD system.
- 16 MB SDRAM—This is the main system memory. This memory is volatile (non-battery backed). During normal operation, it stores the 37XXXD software that is loaded from disk at power-up.
- 8 KB BBRAM—This auxiliary memory chip contains a back-up battery that is continuously recharged whenever power is applied. (The back-up battery has a four year minimum life span.) This chip also contains real time and date clock functions. It is used to store low level boot-up parameters, ALC calibration data, source frequency calibration data, and service log header data.
- 512 KB SRAM—This auxiliary memory is backed-up by a non-rechargeable Lithium battery that provides 200 days (maximum) of power-off protection. It is used to store current and saved front panel setups, trace/normalization data, current RF calibration data, current sweep frequency data, flat power calibration data, and the service log error list.
- VME Bus interface chip—This chip is used to interface the Main Processor PCB to the A13, A14, and A15 digital PCBs (via the VME bus interface).
- SCSI Bus interface—This chip is used to interface the Main Processor PCB to the A16 Hard Disk PCB.

- System boot-up EPROM—This chip contains the boot-up instructions used by the system CPU at power-up.

A13 I/O Interface #1 PCB Assembly

This PCB assembly performs the following functions:

- Floppy drive control—interface for the Floppy Drive Assembly
- External Keyboard control—interface for the front panel Keyboard connector
- Interface for the A18 Rear Panel PCB Assembly (below)
- Interface and control for the rear panel IEEE 488.2 GPIB and Dedicated GPIB interface connectors

A14 I/O Interface #2 PCB Assembly

This PCB assembly contains a State Machine controller, decode logic, and bus interface control circuits that perform the following functions:

- Quiet Bus interface control—The Quiet Bus passes control and data signals from the A9 Main Processor PCB to the A1 through A8, and A21 PCBs and returns status and data signals back to the A9 PCB. This bus is managed by the control circuits on the A14 PCB such that it is inactive during the the time that a measurement is being taken.

> ***NOTE***
> The output data from the A5 PCB A/D converter is sent to the A9 Main Processor PCB via the Quiet Bus, the A14 PCB, and the VME Bus.

- A/D Bus interface control—During the measurement process, all A/D selection and conversion functions on the A5 PCB are controlled exclusively by the A14 PCB State Machine Controller. This is accomplished via the command lines of the A/D Bus.
- Measurement control functions—the A14 PCB State Machine Controller manages many of the VNA functions during a measurement, as follows:
  - Quiet Bus interface control
  - A/D Bus interface control:
    - Sample and Hold control for A5 PCB
    - A/D selection and conversion control for A5 PCB
  - Check for phase lock condition
  - Gain ranging
  - Delay generation for IF Bandwidth setting function

The A14 PCB also provides the interface to the Front Panel A19 and A20 PCBs.

A15 Graphics Processor PCB Assembly

This PCB assembly contains circuitry that simultaneously drives both the LCD display and an external VGA monitor (if used) as follows:

- Receives measurement and display information from the A9 Main Processor PCB and generates screen display (video) information.
- Provides interface and control for the LCD display assembly.
- Provides interface for an external monitor via the rear panel VGA Out connector.

A16 Hard Disk PCB Assembly

The PCB assembly contains a pre-formatted hard disk drive assembly and associated interface circuitry. The A16 PCB interfaces directly with the A9 Main Processor PCB via the (A9) SCSI interface.

Floppy Disk Drive Assembly

This unit is a standard 1.44 MByte DOS compatible format floppy disk drive. It is physically mounted to the test set tray (not to the Front Panel Assembly). It interfaces with the system via the A13 I/O Interface #1 PCB.

A24 VME Bus Terminator PCB

This PCB assembly terminates the VME bus to insure stable digital data transfer on the bus. It plugs into the VME bus structure on the bottom surface of the A17 Motherboard Assembly.

3-5 MAIN CHASSIS ASSEMBLIES

The assemblies described below are the major assemblies mounted to the basic frame of the VNA.

A17 System Motherboard Assembly

The motherboard assembly provides signal routing and D.C. power distribution paths for all major PCB assemblies of the Analog Subsystem (A1 to A8) and the Digital Subsystem (A9 to A16). It also contains the VME Bus, Quiet Bus, A/D Bus structures, and other signal routing paths. It does not contain any active components.

> ***NOTE***
> The motherboard assembly is an integral part of the VNA chassis. It is not a field replaceable unit.

Front Panel Assembly

The Front Panel Assembly consists of the following assemblies and parts:

- A19 Front Panel Switch PCB—this assembly contains all of the front panel switches for the VNA.
- A20 Front Panel Control PCB—this assembly contains the decode logic for the switches located on the A19 Front Panel Switch PCB. This PCB interfaces with the A14 I/O Interface #2 PCB Assembly.
- Front Panel LEDs, beeper, keys, controls, and connectors
- Front panel overlay
- Front panel casting

A18 Rear Panel Interface PCB

This PCB assembly contains the rear panel connectors listed below. It also includes the associated circuitry and cabling interfaces that link these connectors (and the rear panel fan assembly) to the A17 Motherboard PCB and other assemblies within the VNA.

- IEEE 488.2 GPIB connector (with associated interface circuits)
- Dedicated GPIB connector (with associated interface circuits)
- Ethernet RJ-45 Connector
- Printer Out connector (with associated interface circuits)
- VGA Out connector
- I/O Connector (and associated interface circuits)—This 25 pin miniature D-sub connector contains:
  - Limits Testing Status TTL outputs
  - Port 1 and Port 2 Bias inputs.
  - Ext Dig In signal (same as External Trigger BNC)
  - Ext Ana Out signal (same as External Analog Output BNC)

The A18 PCB also contains:

- Routing of –24 Vdc power to the rear panel system fan.
- Routing of External Analog Out and External Trigger Input signals to the Mother Board.

Power Supply Module

The Power Supply Module is a single self contained assembly mounted on the left side wall of the chassis, behind the LCD. This module provides:

- Unregulated +5, +9, ±18, and ±27 Vdc supply voltages to the other assemblies of the 37XXXD
- Thermal and over-current shutdown protection circuitry
- Sensing and input power regulation for operation with 85 to 264 VAC, 48 to 63 Hz, universal AC line input power
- Internal fan cooling (for power supply module)
- Supply voltages distribution

Table 3-1 identifies all 37XXXD DC power supply voltages and lists their usage by the various PCB assemblies. Unless otherwise indicated, supply voltages are regulated on the assembly using them. The analog and digital power supply grounds are isolated.

> ***NOTE***
> All power supply voltages listed in Table 3-1 can be accessed via the A/D bus for measurement by the the A/D converter circuitry (for example, DVM) located on the A5 A/D PCB assembly.

Table 3-1. *37XXXD Power Supply Voltages and Usages*

Voltage	Assemblies Where Used
+5V	A1, A2, A3, A4, A5, A6, A7, A9, A13, A14, A15, A16, A18, A19/A20 (P.O. Front Panel), A21A1/A21A2 (P.O. Source Module), A24, External Keyboard
+9V	A1, A2, A7, A8
+18V	A1, A2, A3, A4, A5, A6, A7, A8, A13
-18V	A1, A2, A3, A4, A5, A6, A7, A8, A13
+27V	A1, A2, A5, A7
-27V	A5, A18
The following supply voltages are derived from the ±18 Vdc supply voltages on the A13 I/O #1 PCB:	
+12V	A9, A15
-12V	A9, A15

Chapter 4
Operational Performance Tests

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Chapter 4
Operational Performance Tests

4-1 INTRODUCTION

The tests in this chapter provide a means of fully testing the 37XXXD VNA system for proper operation and signal stability. These tests are intended to be used as a periodic check of the operational functionality of the VNA.

The tests should be performed in their entirety at least once annually. Although there is no requirement to do so, the tests should generally be run in the sequence presented.

> ***NOTE***
> The procedures presented in Chapter 5, System Performance Verification, provide the means to test the *accuracy* of the measurements performed by the VNA.

Please ensure you have read and fully understand the servicing concepts for the VNA presented in Chapter 1 prior to continuing with this chapter.

Operational tests for the VNA consist of the following:

- Checking the Service Log
- Self Test
- Automated Operational Tests (includes checking the Service Log and Self Test)

These tests are described in Sections 4-2 through 4-5, which start on the next page.

4-2 CHECKING THE SERVICE LOG

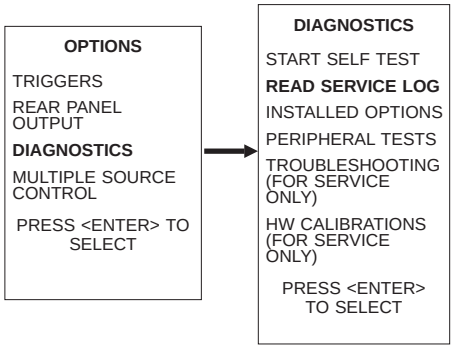
Checking the service log consists of viewing the entries written into the log.

> ***CAUTION***
>
> The service log contains historical information about instrument condition and any failures that may have occurred. It should be cleared only by a qualified service engineer. Such clearing should be accomplished only upon determining that the errors need not be saved to disk, or printed out for service purposes.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu (left); then select **READ SERVICE LOG** from the DIAGNOSTICS menu.



The VNA will now display the contents of the service log. The display consists of a header and an error listing. The header contains a variety of system service information. The error listing contains error messages for failures that may have occurred during operation.

> ***NOTES***
>
> - Errors 7201 to 7209, GPIB remote operation programming errors, report that one or more external GPIB programming errors has been detected. These messages do not indicate a VNA system fault.
> - Informational messages 0000 to 0099 report the pass/fail status of a peripheral access. These messages do not indicate a VNA system fault.

Any other error messages in the service log may indicate an instrument problem and should be investigated. Refer to Chapter 7, Troubleshooting, for further information.

> ***CAUTION***
>
> The **CLEAR SERVICE LOG** menu selection will immediately and permanently clear all the error message entries from the service log. (However, it will not clear the header information.) See Caution message at top of page.

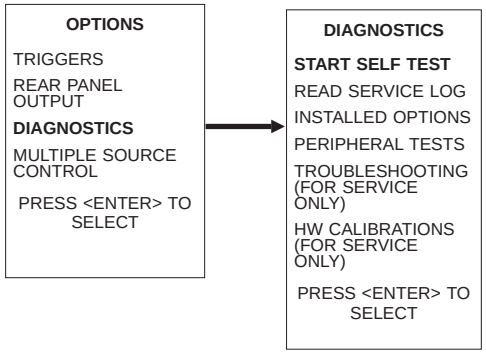
4-3 SELF TEST

The self test performs a series of tests that verify that various internal VNA circuits are functional and operating properly.

To start the self test:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu; then select **START SELF TEST** (below).



Step 3. Wait for test sequence to complete. (Once invoked, this test requires no user interaction or external equipment.)

Upon completion, the net pass/fail result of the self test is shown on the display. If the VNA is in remote-only operation, the results are reported via the GPIB output buffer. If the self test fails, detailed error messages will be written into the service log.

If self test fails:

- ❑ Check the service log to view failure messages.
- ❑ Proceed to Chapter 7, Troubleshooting.

4-4 PERFORMANCE TESTS

The 37XXXD performance tests are contained within one executable program (3700TEST.EXE), Anritsu Software Part Number 2300-178. This includes approximately 15 different tests that cover nearly all of the RF devices and circuits within the VNA and is applicable for all 37XXXA/B/C/D model instruments.

The user interface consists of a single display from which the operator can control all aspects of the test program. It is suggested that the tests be performed in the sequence that they are shown on the display (top-to-bottom sequence), but this is not required. Any test may be performed multiple times or in any sequence. These tests should be performed prior to the verification tests described in Chapter 5, System Performance Verification.

The test program determines the model of the VNA and displays the applicable tests. One general test record and several data files will be created on the PC in a folder labeled 37000. This general test record records only Pass, Fail, Not Applicable, or Not Performed for each test. Other data files will record numerical data, if you so choose. All data files are readable and printable by a text reader such as Notepad.

Each test displays instructions for the operator. Some tests will prompt the operator for frequency characteristics of external test equipment connected.

Test Specifications

Specifications are clearly labeled as being “Typical” or “Guaranteed.” The following tests have specifications that are guaranteed (repairable at no charge by Anritsu during the warranty period):

- Low Power Phase Lock
- Port 1 Power
- Source Match
- Directivity
- System Dynamic Range

All tests that are designated guaranteed allow the operator to store numerical test data to a file. Tests having guaranteed specifications must be performed under test program control.

Specifications that are typical are identical to factory specifications for new instruments. Anritsu does not guarantee the VNA will meet these specifications. If a test fails by a small margin, this does not indicate a problem with the instrument.

Required Equipment

- Windows-based PC with Windows 95 or higher.
- National Instruments GPIB interface card and associated software driver compatible with the installed Windows operating system.
- Standard GPIB interface cable, such as Anritsu part number 2100-2, must be connected between the VNA and the PC.
- Anritsu 365X calibration kit that matches the test port connectors of the VNA must be used. A sliding termination is required only if the Source Match or Directivity tests are to be performed. Only the female components of the calibration kit will be used.
- High quality RF cable suitable for the frequency range of the instrument. Anritsu 3670 or 3671 series throughlines are strongly recommended.
- High quality female to female adapter, such as Anritsu part number 33KFKF50B. Necessary if the above cable does not have a female connector on both ends.

> ***NOTE***
> SMA adapters (with a white teflon dielectric) are too poor in quality even for the lowest frequency VNAs.

Additional Required Equipment

- The Frequency Accuracy test requires an EIP brand frequency counter. Most models are acceptable, but GPIB, Band 3, and External 10 MHz reference input capabilities are required.
- The Port 1 Power test requires an Anritsu model ML24XX power meter with an appropriate power sensor. Other meters and sensors, as shown in Table 1-1, are also useable.
- The Source Match test requires an Anritsu Assurance Airline, such as model T2023-2 or T2025-2, typically available only from Anritsu Service Centers.
- The Directivity test requires an Anritsu Assurance Airline and offset termination, such as model 29KF50-15 or SC4417, typically available only from Anritsu Service Centers.

Installation and Launching the Test Program

The program is a stand alone executable requiring that the National Instruments GPIB software parameters all be set to default conditions. The user will be asked to create the folder “C:\37000” for data storage, if that folder does not already exist on the PC. Additionally, the GPIB settings that are required for the 2300-496 Verification Software will also work with the 3700TEST.EXE program.

From your Windows-based PC, run the program (3700Test.exe). The program's interface will appear similar to the display below:

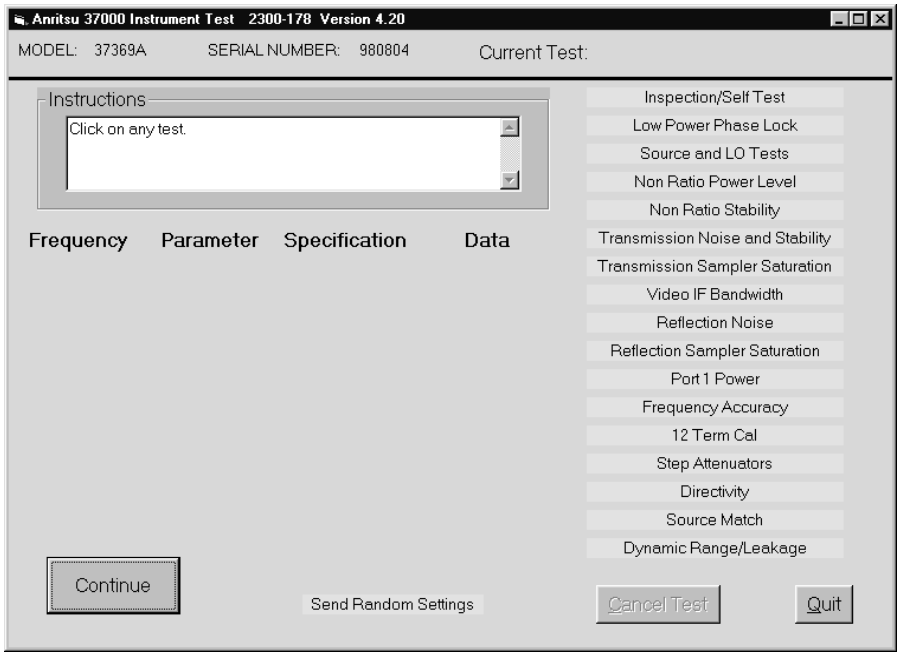


Figure 4-1. *2300-178 Software Interface*

Connect the GPIB cable between the PC and the upper GPIB connector of the VNA rear panel (labeled IEEE 488.2 GPIB). Turn on the VNA and verify the instrument address is 6 (found under the Utility Menu Key |GPIB ADDRESSES).

The Program will locate the VNA, and query the operator regarding his/her name, customer name, and Test Port type.

The program will create a file for Pass/Fail information named "123456.SVC" (where 123456 is the serial number of the VNA). If the program locates an existing .SVC file of the same instrument in the 37000 folder, the operator must decide whether to continue storing data to the existing .SVC test record or start a new .SVC record.

Labels of incomplete tests have a yellow background. A green background indicates that the test passed; a red background indicates that the test failed. (Some versions of the program do not use red to indicate failed tests.)

Running the Tests

To launch any test, simply click on the label of the test. In all tests, except the Front Panel floppy drive test, the operator should not remove the instrument from the Remote condition. Doing so will require restarting the program.

The text box will display instructions to the user. To continue with any test, click on the Continue button, press the space bar, or press <Enter>. To quit any test, press the <ESC> key or click on the Cancel button.

At the completion of the selected test, a Pass or Fail result will be displayed in the text box and written to the .SVC file. If the operator has chosen to record numerical data, it will be saved to the appropriate file. Select Continue to move to the next test.

Description of Tests

Inspection/Self Test:

This test performs the extended internal self test, launches the VNA front panel keyboard/knob test, starts the external keyboard test, and guides the user through a floppy drive test. It also prompts the user to check the pin depth of the Test Ports and to check the fuses in the bias tee circuits.

Low Power Phase Lock:

This test checks the ability of the instrument to maintain source phase lock at minimum source power.

If the test fails, performing a Source Lock Threshold calibration may solve the problem. If this does not solve the problem, it must be corrected by a trained Anritsu Service Engineer.

Source and LO Tests:

These tests use built-in VNA diagnostics to check all phase lock loop error voltages of the RF source, LO1, and LO2 of the down conversion section. Each display should fall within the prescribed limit lines.

If the test fails, a minor deviation outside of the limit lines will not cause any performance problem or measurement error. Performing a new Source Frequency calibration, LO1 calibration, or LO2 calibration will typically bring these voltages back into optimum range.

Non-Ratio Power:

This test checks the RF power level of the four individual RF paths in the VNA. The complete paths are checked beginning with the RF source and continuing out of the VNA Test Ports through the Down Conversion and A/D circuits. All signal paths, including the front panel Option 15 cables (if installed) are tested.

If the test fails and depending on the severity of the power loss, the RF Source in the VNA may fail to phase lock (in worst cases) or the VNA's system dynamic range may be degraded. Ensure the the RF cable between the Test Ports is of good quality and all external cables are connected properly. If this does not solve the problem, it must be corrected by a trained Anritsu Service Engineer.

Non-Ratio Stability:

This test checks the general stabilty of the Non-Ratio channels. Raw data is displayed, stored to memory, then divided by itself resulting in a very smooth RF display at high resolution. The quality of this display is checked after 10 sweeps.

If the test fails, a problem seen in both Test Channels (channels 2 and 3 on the VNA) could be caused by a defective RF cable between the Test Ports. A problem seen on only one channel could be caused by a damaged or incorrectly connected Option 15 front panel cable. A problem seen on all four channels could be caused by an insufficient warm-up period. If the problem still exists after these checks, it must be corrected by a trained Anritsu Service Engineer.

Transmission Noise and Stability:

This test displays the system noise while measuring the default source power (+5 dBm to –15 dBm, depending on model). A short drift test is also performed, testing both Log Magnitude and Phase. The instrument must not be disturbed during the drift test.

If the test fails, the RF cable between the Test Ports is the most likely cause of failure when the problem appears in both S21 and S12. If only S21 or S12 fails, check the Option 15 front panel cables (if installed), then contact a trained Anritsu Service Engineer.

Transmission Sampler Saturation:

This test ensures that the Samplers of the Down Conversion module are operating within their linear range by checking at default and reduced VNA power.

If the test fails, interior attenuators on the VNA RF deck may have been removed or be the incorrect values. The sampler(s) may have degraded requiring replacement of the Sampler/Down Conversion module.

Video IF Bandwidth:

This performs a test on each IF bandwidth filter found on the A4, A3, and A6 PCBs. The operator must perform a Transmission-Only calibration using the calibration kit.

If the test fails in both S21 and S12, the A4 board is suspect. If only S21 fails, the A6 board is suspect. If only S12 fails, the A3 board is suspect.

Reflection Noise:

This is identical to Transmission Noise and Stability except that full reflections are installed on the Test Ports, rather than an RF cable.

If the test fails, check the Option 15 front panel cables (if installed), then contact a trained Anritsu Service Engineer.

Reflection Sampler Saturation:

This test ensures that the Samplers of the Down Conversion module are operating within their linear range by testing with default and lowered source power.

If the test fails, interior attenuators on the VNA RF deck may have been removed or be the incorrect values. The sampler(s) may have degraded requiring replacement of the Sampler/Down Conversion module.

Port 1 Power:

This test measures the RF power present at Port 1 using the VNA default power setting. An Anritsu ML24XX power meter with the appropriate sensor is required. The power data are taken every few hundred MHz, depending on VNA model, so that the test time is 3 to 5 minutes. Data will be written to a file if the operator specifies to do so.

If the test fails, the results may be improved by performing a Port 1 ALC calibration. If this solves the problem, a Port 2 ALC calibration and Source Lock Threshold Calibrations should also be performed. If the test continues to fail, it must be corrected by a trained Anritsu Service Engineer.

Frequency Accuracy:

This test checks the frequency accuracy of the VNA source. An RF counter with several features is required (see Additoinal Required Equipment at the beginning of this section). A precision 10 MHz reference signal (such as that found on an Anritsu MG369XA series synthesizer) should be connected to the rear panel of the counter. Do not use the 37XXXD 10 MHz OUT as a reference for the counter.

If the test fails, it is likely that the VNA's internal 10 MHz crystal has drifted. If a precision 10 MHz signal is present on the counter, the VNA's 10 MHz crystal can be adjusted. The VNA's 10 MHz crystal is mounted on the top of the A7 PCB and is adjustable with a potentiometer. The 10 MHz OUT connector on the rear panel of the VNA provides the access point for monitoring the frequency of the VNA's 10 MHz crystal. After crystal re-adjustment, re-run the Frequency Accuracy test. If the test still fails, the following calibrations will need to be performed (in this order):

1. Source Frequency Cal
2. Port 1 ALC Cal
3. Port 2 ALC Cal
4. Source Lock Threshold Cal

12 Term Cal:

This is a standard OSL measurement calibration, which is required to perform most of the subsequent tests (Step Attenuators, Directivity, Source Match, and System Dynamic Range). The appropriate Anritsu calibration kit with a high density coefficients disk is required. The program selects specific frequencies, using discrete fill, and selects other settings for the calibration required by the System Dynamic Range test. The user must have a female sliding termination if the Directivity or Source Match will be tested.

After the calibration is set up by the program, the operator performs the calibration by connecting the required devices and pressing Enter on the VNA to begin the measurement. After the calibration is complete, the operator selects Continue on the program display and the calibration is saved to the VNA's hard drive. Saving the calibration to the hard drive allows the user to perform other tests (which default the VNA) at any time and recall the calibration as needed.

Step Attenuators:

This will test the accuracy and repeatability of the internal step attenuators. The 12-term calibration must have been performed using the program. This calibration file will be recalled from the VNA's hard drive by the program.

If the test fails, minor failures may occasionally be improved simply by stepping the attenuators up and down for a few minutes to remove oxidation from internal contacts. Major failures of the step attenuators are primarily caused by faults within the attenuators themselves, or perhaps the A8 PCB.

Directivity:

As stated above, the following are required before performing this test:

- Sliding Load calibration performed under control of the 12 Term Cal Test
- Assurance Airline
- Offset Short

Ensure that no RF cables are attached during the test. The assurance airline and offset short are typically available only from Anritsu Service Centers. The test program will use the ripple extraction technique to derive the corrected directivity of both Test Ports. Numeric data may be saved.

If the test fails, ensure that the pin depth of the Test Ports are within specification and that the center pins are not misaligned. The coupler or bias tee for each Test Port is also a possible cause of failure.

Source Match:

The following is required to perform this test:

- Sliding Load calibration performed under control of the 12 Term Cal Test
- Assurance Airline
- Short

Ensure that no RF cables are attached during the test. The assurance airline is typically available only from Anritsu Service Centers. The test program will use the ripple extraction technique to derive the corrected source match of both Test Ports. Numeric data may be saved.

If the test fails, ensure that the pin depth of the Test Ports are within specification and that the center pins are not misaligned. The coupler or bias tee for each Test Port is also a possible cause of failure.

System Dynamic Range:

Software for this test is currenly under development. Contact Anritsu Customer Service for availability.

Send Random Settings:

This test sends random start and stop frequencies and reduces source power in an attempt to expose intermittent failures. If failures occur, details are written to the VNA's service log for evaluation by a trained Anritsu Service Engineer. This test will continue indefinitely until stopped by the operator (using the Escape key or Cancel button) or when 20 errors have occurred.

If the test fails, due to the extreme nature of this test, a very intermittent error may appear (for example, once in several days), which cannot be duplicated by manual testing. If this is the case, it may or may not be prudent (in the view of the user) or successful to attempt a repair. If several errors appear in one day, a significant problem exists and a repair should be performed by an Anritsu Service Engineer.

4-5 LOG MAGNITUDE DYNAMIC ACCURACY TEST

This test verifies the measurement accuracy of the VNA at power levels that are significantly below 0 dBm. An external step attenuator that has been accurately characterized at the Anritsu Calibration Lab is used. S21 only measurements at 2.0 GHz will be performed manually at each step of the attenuator. Uncertainty associated with the step attenuator and characteristic VNA uncertainty are part of the criteria used in the Pass or Fail determination for each attenuation step.

If the S21 measurement data for the attenuation value is within the allowable uncertainty, the VNA is measuring within factory specification for that power level.

A test record with pre-calculated uncertainties is shown in Table 4-1. This test record should be copied before use.

Required Equipment

The following equipment is required for the Log Magnitude Dynamic Accuracy Test:

- Anritsu SC5567 (consisting of Model 4622K Step Attenuator with Characterization Disk)
- Anritsu SC3796 Step Attenuator Controller (uses standard 9-Volt batteries)
- Anritsu Model 3652 or Model 3652-1 Cal Kit Including Phase-equal Adapters
- Anritsu Throughline (qty. 2) to fit the VNA test ports
- If the VNA has V connector test ports (50 or 65 GHz models), V-to-K adapters will be required to convert the test ports from V connectors to K connectors

Test Procedure

> ***WARNING***
> Incorrectly installing the step attenuator into the driver fixture will damage the step attenuator. Carefully follow the directions specified below:

Step 1. Default the VNA.

Step 2. Install a test cable to both Port 1 and Port 2 (with V-to-K adapters on the cables if the VNA has V connector test ports). Highest quality measurements will be obtained if phase-equal insertable adapters from the cal kit are used at the measurement end of the cables (and changed as necessary during calibration and measurement).

Step 3. Press the Utility Menu key and select:
Cal Component Utilities.

Step 4. Insert the floppy disk from the cal kit into the VNA and select **Install Kit Information From Floppy Disk**.

Step 5. Press the Begin Cal key and set up a CW calibration with the following parameters:

- Full 12 Term
- Include Isolation
- CW 2.0 GHz
  (use the **Discrete Fill** menu to set to 2.000 GHz)
- Connector Type: K male for both ports
- Load Type: Broadband

Step 6. Install the Broadband Loads at the Isolation Device measurement step. Before measuring the Isolation Devices, make the following changes:

- Press the AVG/Smooth menu key
- Set averages to **4096 (x1)**
- Press the Video IF BW key
- Select **Minimum 10Hz**
- Press <Enter> to measure the Isolation Devices.

Step 7. Before measuring the Broadband Loads (at the Broadband Load measurement step):

- Turn on **4096** averages
- Set IF Bandwidth to **Minimum (10 Hz)**.

Step 8. Complete the calibration using default settings for other devices.

> ***WARNING***
> Incorrectly installing the step attenuator into the driver fixture will damage the step attenuator. Read the following step carefully.

Step 9. Observe the white dots and/or beveled connector corners that designate Pin 1 on the driver fixture and the attenuator ribbon cable plug, then plug the ribbon cable into the socket of the fixture so that the Pin 1 dots or beveled corners are aligned together. (The switches on the driver fixture are used to activate different attenuation steps.)

Step 10. Install the 4622K step attenuator and press the Data Points key, then enter **10 Points Drawn in CW**.

Step 11. For an attenuator setting greater than 30 dB, set averages to **4096**, turn on averaging by pressing the Average key, and then set the IF Bandwidth to **Minimum (10 Hz)**.

Step 12. View the S21 measurement display at a moderately high degree of resolution.

Refer to Figure 4-2 (page 4-19) for a typical example measurement. In this case, the step attenuator is set to the 70 dB setting. Note that the VNA produces an average measurement of approximately -70.05 dB.

It will be useful to print each attenuation display using the CaptureVNA program (found on the VNA Utilities CD shipped with each VNA) or another method.

Analysis of the Measurement

A visual estimate of the average value of the data points is sufficient for the purposes of this test. Record the (visual) average value for each attenuation step in Column B of Table 4-1 (page 4-19).

Open the data file (using a text reader program) on the Characterization Disk of the step attenuator. The data for each attenuation step is found on the same line as the nominal attenuation value. For example, assume the line reads “10= -10.02,0.05”. Copy “-10.02” to Table 4-1 in Column C. Do not record the value of “0.05”, which is the uncertainty of that step. Transfer the 8 characterization values to Column C.

The uncertainty values in Column D of Table 4-1 are derived values that are a composite of the uncertainty of the VNA and the uncertainty of the step attenuator. Add the values of Column C to Column D to compute the values for the Upper Limit. Record the computed values in Column E.

Subtract the values of Column D from Column C to compute the values for Lower Limit. Record the computed values in Column F.

If the measured value in Column B falls between the values of Columns E and F, the attenuation test passes (Column G). If the Column B value is outside the Columns E and F values, the attenuation test fails.

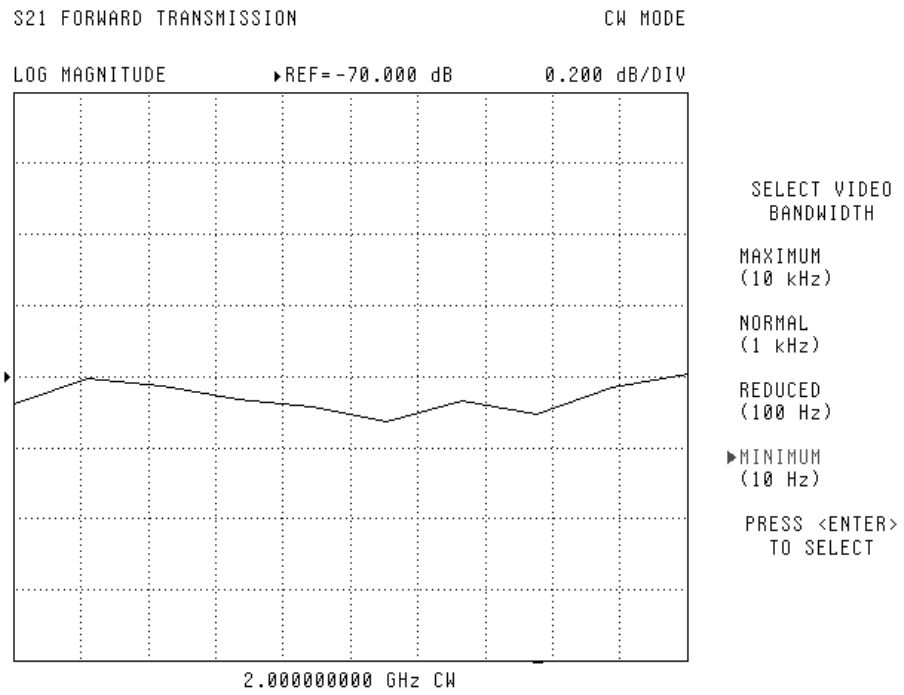


Figure 4-2. *Log Magnitude/Dynamic Accuracy Test Result*

37XXXD Log Magnitude Dynamic Accuracy Test

Model:_____ Serial Number:_____ Date:_____

Operator:_____ Step Atten. ID:_____

--A-- Attenuation Device Nominal Value	--B-- Measured Value (Avg)	--C-- Attenuation Device Characterized (or Traceable) Value	--D-- Composite Uncertainty	--E-- Col. C + Col. D (Upper Limit)	--F-- Col. C - Col. D (Lower Limit)	Pass or Fail
–10 dB			0.107			
–20 dB			0.105			
–30 dB			0.106			
–40 dB			0.105			
–50 dB			0.156			
–60 dB			0.210			
–70 dB			0.330			
–80 dB			0.597			

Table 4-1. *Log Magnitude/Dynamic Accuracy Test*

Chapter 5
System Performance Verification

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Chapter 5
System Performance Verification

5-1 INTRODUCTION

This chapter provides specific procedures to be used to verify that the VNA is making accurate, traceable S-parameter measurements. The operational performance tests described in Chapter 4 should be performed at least once anually, and prior to verifying the system performance test procedures in this chapter.

Please ensure that you have read and fully understand the servicing concepts for the VNA presented in Chapter 1 prior to continuing with this chapter.

The ME7808B/C broadband system verification is described in Appendix D.

5-2 CALIBRATION AND MEASUREMENT CONDITIONS

The surrounding environmental conditions and the condition and stability of the test port connectors, through-cable, and calibration kit determine the system measurement integrity to a large extent.

These are all user controlled conditions, and as such, should be evaluated periodically for impact on system performance. If these conditions vary significantly with time, the system verification procedures should be performed more often than the recommended annual cycle.

Standard Conditions

The standard conditions specified below must be observed when performing any of the operations in this chapter—both during calibration and during measurement.

- Warm-up Time:
  One hour minimum
- Environmental Conditions:
  Temperature: 23 ±3 deg C
  Relative Humidity: 20% to 50% recommended
- Error Correction:
  Perform software-guided 12-term calibration

Special Precautions When performing the procedures in this chapter, observe the following precautions:

- Minimize vibration and movement of the system, attached components, and through-cable.
- Clean and check the pin depth and condition of all adapters, through-cable(s), and calibration components.
- Pre-shape the through-cable(s) so as to minimize their movement during calibration and measurement activities.

5-3 MEASUREMENT ACCURACY

The verification procedures described in the following sections verify the published measurement accuracy and measurement traceability* for the VNA.

Verification Software These procedures require the use of the VNA Verification Software package that is included in the Verification Kit. See Table 1-1 for software part numbers. The Standard Conditions and Special Precautions described in Section 5-2 should be observed when performing these procedures.

The verification software performs the following functions:

- It guides the user through a full 12-term calibration of the VNA.
- It guides the user through measurements of the S-parameters of the NIST traceable standards (below).
- It verifies that the measured values are within the specified measurement uncertainty limits.
- It indicates the pass/fail status of the measurements on the display.
- It can also provide a hard copy printout of the measured data, measurement uncertainties, and the standards used.

> ***NOTE***
> The total verification uncertainty in these VNA measurements includes the measurement uncertainty of the verification standards and the uncertainty of the VNA itself.

* Traceability to the U.S. National Institute of Standards and Technology (NIST)

Verification Result Determination

The software verification process compares the measured S-parameter data of the standards against the original standard data for those devices that was obtained using the Factory Standard 37XXX Vector Network Analyzer System (at Anritsu). The factory Standard 37XXX system is traceable to NIST through the Anritsu Calibration Laboratory's Impedance Standards. These standards are traceable to NIST through precision mechanical measurements, NIST approved microwave theory impedance derivation methods, and electrical impedance comparison measurements.

The quality of the verification results is very dependent on the degree of care taken by the user in maintaining, calibrating, and using the system. The most critical factors are:

- The stability and quality of the devices in the calibration and verification kits.
- The condition of the VNA test port connectors and through cables.
- The pin depths of all connectors and the proper torquing of connections. These same factors also affect the VNA's measurement quality.

Consult the Operating Manuals supplied with the Anritsu Calibration and Verification Kits for proper use, care, and maintenance of the devices contained in these kits.

5-4 VERIFICATION PROCEDURE

The performance verification procedure for the Anritsu 37XXXD VNA is described below. The Software Users Guide (embedded within the Verification Program) explains in detail the procedures to be used for the installation and operation of the Verification Software on your computer/controller.

Equipment Required:

- Anritsu 3700 Verification Software (included in the Verification Kit for the connector type in use; refer to Table 1-1)
- External computer/controller; refer to Table 1-1
- Anritsu Calibration Kit identical to the Test Port connectors of the VNA; refer to Table 1-1
- Anritsu Verification Kit identical to the Test Port connectors of the VNA; refer to Table 1-1
- GPIB cable (Anritsu PN: 2100-2), or equivalent
- Anritsu Test Cable Model 3670K50-2 or 3670V50-2 or equivalent

> ***NOTE***
> Use of non-Anritsu calibration or verification kits is not supported.

Procedure:

Step 1. Using the GPIB cable, connect the external computer/controller to the IEEE 488.2 GPIB Interface port on the VNA's rear panel.

Step 2. Insert the CD ROM into the computer's drive and install the verification software.

Step 3. Follow the directions displayed on the computer screen to perform all tests.

If any failures are indicated, check the connectors of the calibration kit devices and the impedance transfer standards for damage, cleanliness, proper connection, and torquing. These are the most common causes for verification failures.

If failures persist, run all of the tests in the 2300-178 program, described in Chapter 4.

5-5 VNA TRACEABILITY

According to the *International Vocabulary of Basic and General Terms in Metrology (VIM), BIPM, IEC, IFCC, ISO, IUPAC, IUPAP, OIML*, 2nd ed., 1993, definition 6.10, traceability is defined as the property of the result of a measurement or the value of a standard that can be related to *stated references* through an *unbroken chain of comparisons* all having *stated uncertainties.*

The *stated references* are *stated reference standards. Stated* means explicitly set forth in supporting documentation. *Reference standard* is a standard generally having the highest metrological quality available at a given location or in a given organization from which measurements are derived. The *stated references* are usually national or international standards.

The *unbroken chain of comparisons* are the complete, explicitly described, and documented series of comparisons that successively link the value and uncertainty of a result of a measurement with the values and uncertainties of each of the intermediate reference standards to the highest reference standard of which traceability for the result of measurement is claimed.

The *stated uncertainties* are the uncertainties of measurement that fulfill the VIM definition as the parameter and is associated with the result of a measurement that characterizes the dispersion of values that could reasonably be attributed to the measurand. The stated uncertainty is evaluated and expressed according to the general rules given in the *ISO Guide to the Expression of Uncertainty in Measurement*.

The Vector Network Analyzer (VNA) is one of the most modern and accurate measurement tools for microwave and RF applications, but VNA requires calibration to enhance its measurement accuracy. There are many ways to define proper measurement traceability for the VNA in lieu of its system complexity and calibration schemes. Scattering Parameters (S-Parameters) are the most common measurands of the vector network analyzer.

In the chart below, a widely used traceability path for making scattering parameter measurements is presented. The basic elements in this chart include a calibration kit, a VNA, and a verification kit for each user. The calibration kit is characterized and traceable mainly through impedance standards, for example airlines and proper circuit modeling.

The vertical path is a process that is used by most of the manufacturers and primary standards laboratories. It is impractical for regular users to demonstrate the system traceablity before every use; therefore, a verification kit consisting of an airline, mismatch airline, and two fixed attenuators was introduced to perform a routine check for the calibrated system. These components were characterized by their manufacturers or by a standards laboratory, and they have excellent repeatability characteristics.

The horizontal path shows the conventional traceability chain for the verification kit. The stated uncertainty in the verification program comes from three major sources:

- NIST Report
- Anritsu Reference Standards
- Device-under-test

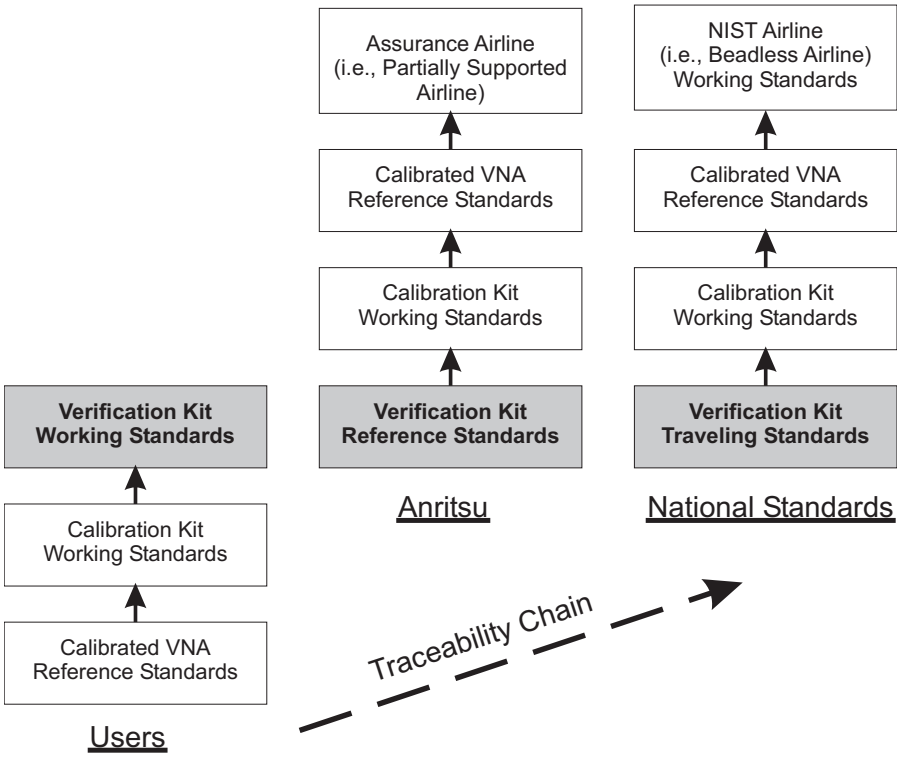

Figure 5-1. *VNA Traceability Chart*

Chapter 6
Adjustments

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Chapter 6
Adjustments

6-1 INTRODUCTION

This chapter contains procedures that are used to restore the calibration of the VNA signal source and the related source lock system assemblies. Use these procedures after various signal source related assemblies have been replaced due to troubleshooting or repair activities.

Please insure that you have read and fully understand the servicing concepts for the VNA presented in Chapter 1 prior to continuing with this chapter.

Saving each new calibration file to the hard drive is suggested in these instructions. This is simply creating a backup copy of the file and is not required.

6-2 LO1 CALIBRATION

This procedure uses the VNA internal diagnostics and calibration menus to adjust the A1 1st LO PCB assembly. Perform this calibation procedure if:

- The A1 PCB is replaced.
- Display of DIAGNOSTICS/TROUBLESHOOTING/LO1 MAIN PHASELOCK VOLTAGE is outside of the limit lines.

Calibration Procedure

Perform the following steps:

Equipment Required:

None

> ***NOTE***
> Allow the VNA to warm-up at least 30 minutes prior to performing calibration.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS** | **LO1 CALIBRATION.**

Step 3. Perform the calibration (it is completed in less than five seconds).

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.LO1.**

If calibration fails:

Step 1. Repeat the calibration.

Step 2. If the calibration fails, replace the A1 PCB and perform the calibration again.

6-3 LO2 CALIBRATION

This procedure uses the VNA's internal diagnostics and calibration menus to adjust the A2 second LO PCB assembly. Perform this calibation procedure if:

- The A2 PCB is replaced.
- Display of DIAGNOSTICS/TROUBLESHOOTING/LO2 MAIN PHASELOCK VOLTAGE is outside of the limit lines.

Calibration Procedure

Perform the following steps:

Equipment Required:

None

> ***NOTE***
> Allow the VNA to warm-up for at least 30 minutes prior to performing this calibration.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS** | **LO2 CALIBRATION.**

Step 3. Perform the calibration (it is completed in less than five seconds).

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If the calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.LO2.**

If the calibration fails:

Step 1. Repeat the calibration.

Step 2. If the calibration fails, replace the A2 PCB and perform the calibration again.

6-4 FREQUENCY CALIBRATION

This procedure uses the internal VNA diagnostics and calibration menus, in conjunction with a suitable frequency counter (refer to Table 1-1), to adjust the signal source frequencies throughout the range of the VNA model being calibrated. Perform this calibration procedure if:

- The Source FM/Lock Linearity test in Chapter 4, Operational Performance Tests, fails.
- Other testing or troubleshooting reveals a possible problem with the signal source frequency accuracy or phase lock loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller
  - Down Converter
  - YIG Oscillator
  - Switched Filter
- BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

Calibration Procedure

Perform the following steps:

Equipment Required:

Refer to Table 1-1 for further information about the following equipment:

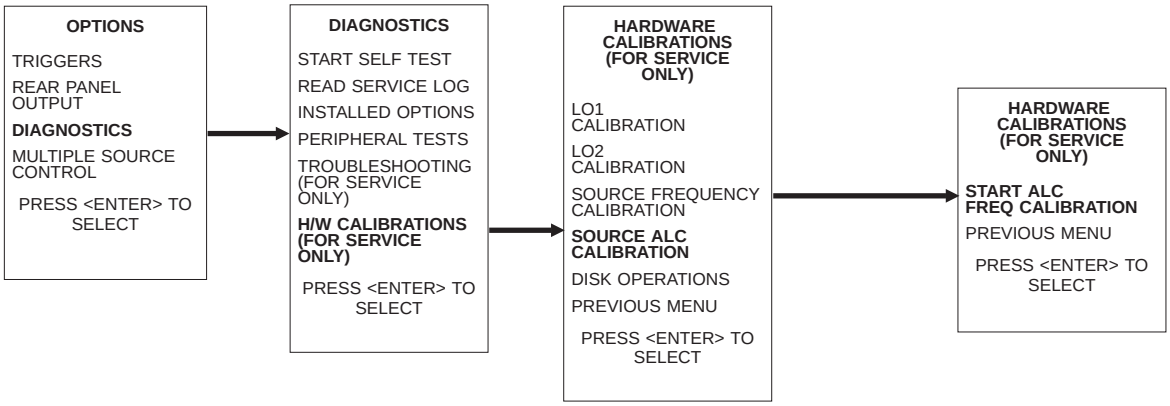
- Anritsu MF241XB Frequency Counter or equivalent EIP brand counter equipped with Band 3 Input and GPIB capability
- RF/Microwave Cable
- GPIB cable (Anritsu 2100-2, or equivalent)

> ***NOTE***
> Allow the VNA and Frequency Counter to warm-up for at least 30 minutes prior to performing this calibration.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATION** | **SOURCE FREQUENCY CALIBRATION** (below).



Step 3. Follow the directions displayed on the screen to set-up and connect the frequency counter to the VNA. Refer also to Figure 6-1. Select **START SOURCE FREQ CALIBRATION** from the menu (above).

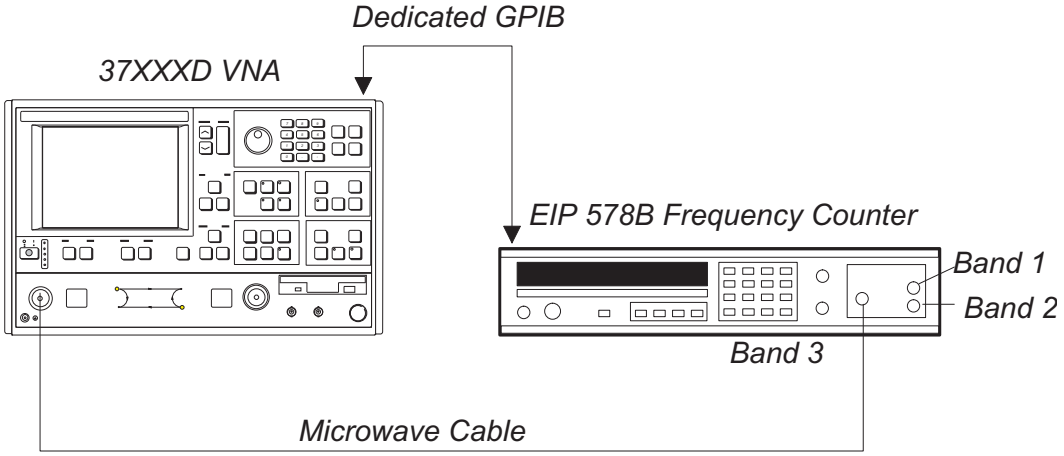


Figure 6-1. *Test Setup for Frequency Calibration*

Step 4. Follow the directions displayed on the VNA screen until the calibration is completed.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.FRE.**

If calibration fails:

- Verify that the GPIB cable is connected to the Dedicated GPIB (bottom) connector on the VNA's rear panel.
- Verify that the frequency counter is functioning correctly, the cable is in good condition, and all connections are secure.
- Repeat the calibration. If it still fails, then go to Chapter 7, Troubleshooting.

6-5 RF POWER/ALC CALIBRATION

This procedure uses the VNA's internal diagnostics and calibration menus, in conjunction with a suitable power meter, to adjust the output power level of the signal source throughout the range of the VNA model being calibrated. Perform this calibration procedure if:

- The Port 1 Power test in Chapter 4, Operational Performance Tests, fails.
- Other testing or troubleshooting reveals a possible problem with the RF Power accuracy or the ALC loop.
- Any of the following assemblies are replaced:
  - A21A1 Source YIG/Bias
  - A21A2 Source Controller
  - Down Converter
  - YIG Oscillator
  - Switched Filter
  - Transfer Switch
  - SDM or SQM
  - Coupler
  - Port 1 Source Step Attenuator
- The BBRAM chip on the A9 Processor PCB is replaced and the Source Calibration Data was not previously saved on disk (thus data could not be recalled from disk).

Calibration Procedure

Perform the following steps:

Equipment Required:

Refer to Table 1-1 for further information about the following equipment:

- Anritsu ML24XXA with Version 2.02 or later, with Anritsu Power Sensors MA2474A (use sensor SC6230 for 50 and 65 GHz models)
- GPIB cable (Anritsu 2100-2, or equivalent)

> ***NOTE***
> Allow the VNA and power meter to warm-up for at least 30 minutes prior to performing this calibration.

Procedure:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from menu, then select in sequence: **H/W CALIBRATIONS | SOURCE ALC CALIBRATION** (next page).

Step 3. Follow the directions displayed on the screen to set-up and connect the power meter to the VNA. Refer also to Figure 6-2. Select **START ALC CALIBRATION** from the menu.

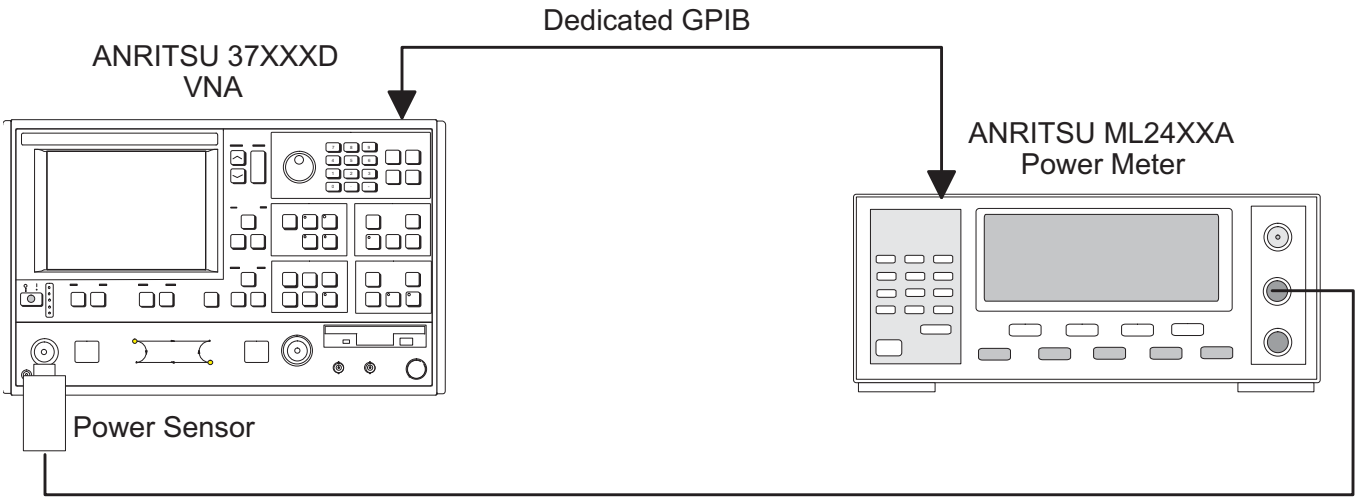


Figure 6-2. *Equipment Set-Up for RF Power / ALC Calibration*

Step 4. Follow the directions displayed on the VNA screen until the calibration is completed.

Step 5. When Port 1 has been calibrated, connect the Power Sensor to Port 2 and Calibrate Port 2.

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | DISK OPERATIONS | SAVE TO HARD DISK | HW_CAL.ALC.**

Perform the Port 1 Power test in Chapter 4, Operational Performance Tests. If the test fails, proceed to Chapter 7, Troubleshooting.

If calibration fails:

- Verify that the GPIB cable is connected to the Dedicated GPIB (bottom) connector on the VNA's rear panel.
- Verify that the power meter and sensor are functioning correctly, the cables are in good condition, and all connections are secure.
- Verify the correct power sensor data exists in the power meter.
- Repeat the calibration. If it still fails, then proceed to Chapter 7, Troubleshooting.

6-6 SOURCE LOCK THRESHOLD

This procedure uses the VNA internal diagnostics and calibration menus to adjust the source lock threshold of the phase-lock loop. Perform this calibation procedure:

- If the Low Power Phase Lock Test (Chapter 4) fails.
- Anytime the Port 1 ALC Calibration is done.
- If the A4 PCB is replaced.
- If the A8 PCB is replaced.
- If the BBRAM chip on the A9 Processor PCB is replaced and the Source Lock Threshold calibration data was not previously saved on disk (that is, data is not available for recall from a floppy disk).
- If the Sampler/Down Conversion Module is replaced.

Calibration Procedure

Perform the following steps:

Equipment Required:

None

> ***NOTE***
> Allow the VNA to warm-up for at least 30 minutes and perform the ALC calibration (Section 6-5) prior to performing this calibration.

Procedure:

Step 1. If recalibrating a 50 or 65 GHz model , install broadband terminations to both ports or install a throughline between ports.

Step 2. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 3. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS | SOURCE LOCK THRESHOLD CALIBRATION.**

Step 4. Follow the directions displayed on the VNA's screen, until the calibration is completed. (If the instrument is a 65 GHz model, the calibration will take several hours.)

Post Calibration Actions

After the calibration process is completed, perform the following actions, as appropriate:

If calibration passes:

Save the calibration data to (hard) disk, as follows:

Step 1. Press the Option Menu key (Enhancement key group) to display the OPTIONS menu.

Step 2. Select **DIAGNOSTICS** from the menu, then select in sequence: **H/W CALIBRATIONS |DISK OPERATIONS |SAVE TO HARD DISK|HW_CAL.SLT.**

If calibration fails:

Step 1. Repeat the calibration.

Step 2. If the calibration still fails, proceed to Chapter 7, Troubleshooting.

Chapter 7
Troubleshooting

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Many of the troubleshooting procedures presented in this chapter require the removal of instrument covers to gain access to printed circuit assemblies and other major assemblies.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many assemblies in the VNA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

Chapter 7
Troubleshooting

7-1 INTRODUCTION

This chapter provides brief information on most failure modes of the 37XXXD instrument family. Only the most basic repairs should be attempted by non-factory-trained technicians. Insufficient care or training will often result in damage to the instrument and cause increased expense and down time. Note that every Anritsu Service Center has factory-trained Service Engineers who can solve all 37XXXD operation problems quickly and reliably, often with warranted repairs.

Before removing the covers of the 37XXXD VNA, be sure that static safety guidelines are followed as detailed in Section 1-12.

7-2 POWER-UP PROBLEMS

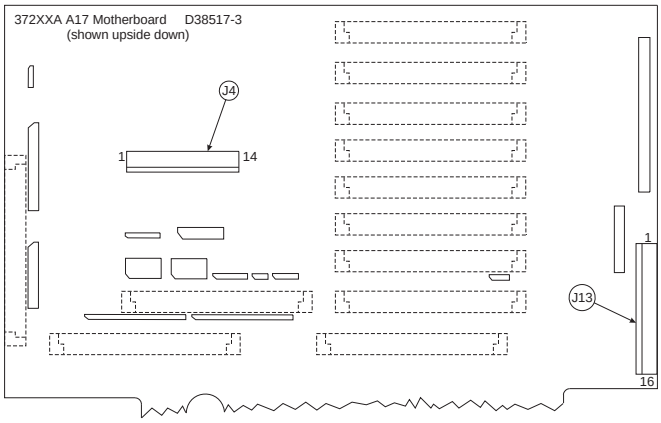
If the instrument is non-functional when power-up is attempted, proceed as follows:

> ***WARNING***
>
> The main power supply for the instrument is mounted on the left side of the instrument chassis. Remove the power cord before attempting to remove this supply. Simply turning off the power is not sufficient because hazardous voltages are present under the clear plastic cover whenever a power cord is in place.

Step 1. Remove the bottom cover as described in Section 8-3.

Step 2. Check the power supply voltages at J4 and J13 of the motherboard. The correct voltages and acceptable AC ripple are listed below:

Table 7-1. *DC Power Supply Voltage Checks*



Connect To:			DC Supply Voltage	AC Ripple and Noise
Conn	Com (Pin)	Meas (Pin)		
J13	8	16	0 Vdc	50 mVpp
J13	8	1	+4.8 Vdc to +5.1 Vdc	50 mVpp
J4	4	2	+9 Vdc +5% / –0%	50 mVpp
J4	4	6	+18 Vdc +5% / –0%	50 mVpp
J4	4	10	–18 Vdc +5% / –0%	50 mVpp
J4	4	12	+27 Vdc +5% / –0%	50 mVpp
J4	4	14	–27 Vdc +5% / –0%	50 mVpp

Figure 7-1. *Location of Connectors for Power Supply Voltage Checks*

Step 3. If the instrument continuously power cycles approximately once per second, it is possible that a PCB or RF component has developed a short. To troubleshoot this type of problem, lift each PCB (one by one) out of its enclosure and try to restart.

Step 4. If a problem PCB is not found, disconnect each RF component by **gently** unplugging the bias connector from the motherboard connector. Do not disconnect RF cables.

Step 5. When the faulty PCB or RF component is disconnected, the VNA will power-up, but other error messages will appear. After the defective assembly is identified, it can then be replaced.

7-3 HARD/FLOPPY DISK AND DISPLAY PROBLEMS

Refer to the following paragraphs for the associated type of problem that you may be having.

Failure to Boot-up from the Hard Disk

If the system does not boot-up from the hard disk, the problem is often solved by booting-up the system from the floppy disk and formatting the hard drive as follows:

> ***WARNING***
> Reformatting the hard drive will erase all saved files. You may continue to boot from floppy disks if deleting these files is not acceptable. A software utility to archive saved 37XXXD files on a PC is available on the Anritsu VNA Software Utilities CD (Anritsu part number 2300-481).

Step 1. Locate the extra set of Operating Software disks that is included with each 37XXXD Operation Manual.

Step 2. Insert Disk 1 into the floppy drive and turn on the VNA.

Step 3. Load the other disks when prompted on the VNA display.

Step 4. After the VNA is operational, the hard drive may be formatted via the **Utility** / General Disk Utilities key sequence. (Note the warning above before formatting).

Step 5. After the drive is reformatted, turn off the 37XXXD, insert Disk 1 in the floppy drive, and load all disks again. The Operating software will be saved automatically to the hard drive.

Step 6. If the problem is not solved using this method, install a new A16 PCB. Detailed instructions are packaged with the replacement A16 PCB.

Floppy Disk Drive Problems

Floppy disk drive problems may be caused by dust buildup, general floppy drive failure, or A13 PCB failure.

Anritsu does not recommend purchasing a replacement drive from sources other than Anritsu since the VNA A13 PCB supports only a limited number of floppy drive types.

Display Problems

The cause of display failures is typically either the A15 PCB, the LCD backlight driver PCB, or the LCD display itself. Replacement part numbers are shown in Chapter 2.

It may be useful to connect an external VGA monitor to the rear panel of the 37XXXD so that the instrument is useable if the LCD display is inoperative. If the external VGA monitor also does not produce a display, then the problem is caused by an A15 PCB failure.

7-4 OTHER BOOT-UP PROBLEMS

As the VNA boots, communication with several subsystems is attempted. If the process stops before boot-up is complete, the last item displayed on the LCD is typically the failing assembly. For example, if the instrument does not boot-up beyond the "Initializing GPIB (A13/A18)" line, then this would indicate a failure of the A13 or A18 PCB.

Error messages having a numerical prefix of 01xx through 21xx indicate which PC board is likely to have failed. For example, "0311 TA IF COMM FAIL" indicates that the A3 PCB is not communicating correctly.

"IF Cal Failure" messages usually require analysis of the Service Log. Refer to Section 7-7, *Error Messages During Measurements.*

Loss of Calibration or Saved Setups After Power-down

If any of the setups shown below are lost after power-cycling, the cause is probably a defective coin-style 3v battery on the A9 PCB. This battery (Panasonic CR2032 or equivalent) is readily available at retail stores.

- Cal LED is out after power-cycling (Cal LED was ON when power was turned off)
- Front Panel setup does not match setup when power was turned off
- Internal Memories (1 through 10) have lost saved setups
- GPIB addresses have changed

Warming Up... Please Wait

This error message indicates that the 37XXXD is not capable of phase locking the RF Source (internal or external) and is displayed only during the first 5 to 10 minutes after turn-on. There are many possible causes for this failure, such as factory recalibrations being overdue, system hardware being setup incorrectly (external RF Source or Millimeter Wave system), or a failed assembly in the instrument. After approximately 10 minutes, if the problem still exists, Lock Failure messages will usually appear. The following checks should be made (in this order):

Step 1. Check all front panel cables on instruments having Option 15.

Step 2. Refer to Appendix D for setup instructions on Millimeter Wave systems.

Step 3. Press **OPTION MENU | RECEIVER MODE** keys and ensure that the mode is set to "Standard."

Step 4. Perform a master reset (**Default Program | 0** keys). Reload the Cal Kit Coefficients disks after this reset.

Step 5. Analyze messages shown in the Service Log. Take note of the date of last calibrations.

Step 6. Troubleshoot lock failure messages as described in this chapter.

7-5 UNDERSTANDING THE SERVICE LOG

The VNA Service Log may be viewed under the **Option Menu** | Diagnostics | Read Service Log key sequence. This log displays general instrument configurations, factory calibration dates, and a list of messages. These messages show instrument problems and other informational messages, such as GPIB programming errors and operator setup problems.

As mentioned in the previous section, error messages having a numerical prefix of 01xx through 21xx indicate which PC board is likely to have failed. For example, "0311 TA IF COMM FAIL" indicates that the A3 PCB is not communicating correctly.

Messages that are labeled "Informational" or those that describe a GPIB command fault or GPIB response time out do not indicate problems with the instrument functionality.

Messages containing the words "Phase Lock Failure" are discussed in Section 7-7.

Messages relating to "warming-up" indicate that the instrument is not source-locking correctly when cold. The 37XXXD is not malfunctioning in this cold condition since the specified warm-up time has not been achieved.

Messages of "RF Unleveled" are frequently caused by the operator setting the RF Source power above Default. To correct this situation, lower the RF power of the Source (**Setup Menu** / Test Signals key sequence). If the message, "RF Unleveled" appears with the Source Power set to 0 dB (Default) or lower, a problem exists with the 37XXXD.

Numerical data with no easily understood identifying labels is of use only to Anritsu Service personnel in the process of PC board repair. PCB repair is a factory-only function.

The following items of information found in the Service Log are highly useful to Service Engineers when troubleshooting errors:

SWP=R or SWP=F
This indicates whether the instrument was in forward or reverse sweep when the problem occurred, and is useful in Phase Lock Failure troubleshooting and RF Unleveled problems.

PWR –x.x
All 37XXXD instruments have default power settings of –7 dBm or above shown under the Setup Menu / Test Signals key sequence.

SYS x.xxxx
This indicates the approximate frequency at which the problem occurred.

<OVL>
This indicates "out-of-range". The internal 37XXXD DVM was not able to measure the voltage. This is particularly useful information when troubleshooting IF Calibration errors.

7-6 DIAGNOSTIC DISPLAYS

The Diagnostic displays listed below are useful in troubleshooting the 37XXXD problems to the replaceable subassembly level. These displays are found under the **Option Menu** / Diagnostics / Troubleshooting key sequence. Other troubleshooting displays are for component-level troubleshooting by factory technicians only.

- Non-Ratio Parameters
- LO1 Phase Lock Voltage
- LO2 Main Phase Lock Voltage
- Source Linearity Voltage
- GPIB Test (found under the **Diagnostics** / Peripheral Tests menu key sequence)

These displays are identical to those shown automatically in the 2300-178 Operational Tests program described in Chapter 4. Information regarding failures of each test is also included in Chapter 4.

After the desired tests have been performed, the user must select "Finished, Recover from Troubleshooting" or press the Default Program key to exit this mode.

7-7 ERROR MESSAGES DURING MEASUREMENTS

Lock Failure D or DE (60xx)

The Lock Failure D or DE error message indicates that the source phase locking circuits are not operating. If the instrument is fitted with Option 15, check all of the front panel cables connected in the "a1" and "a2" RF paths. Occasionally , this problem may be solved by performing new recalibrations as described in Chapter 6. If the condition persists, the difficult nature of this problem means that the 37XXXD should be returned to an Anritsu Service Center where factory-trained Service Engineers and replacement parts are available.

> ***NOTE***
> If the error message also contains the prefixes A, B, or C, the corrective action is found in paragraphs farther down in this section.

The following additonal information sources are useful to solve this problem:

- Service Log Information
- Troubleshooting Flowcharts (Figures 7-2 or 7-3)
- Block Diagrams for the Source Lock Paths Found in Chapter 3
- DC Voltage Tables 7-2 through 7-4
- Power Meter
- DC Voltmeter
- Oscilloscope
- Spectrum Analyzer

Other Lock Failures

Lock Failure A, B...

The “A” indicates a failure of the 10 MHz system clock and all other prefixes and error messages are a result of the 10 MHz clock failure. Replace the A7 PCB.

Lock Failure B, D, E

This indicates that the LO1 (A1 PCB) has failed. Replace the A1 PCB and recalibrate the LO1 as described in Chapter 6.

Lock Failure C, D, E

This indicates that the LO2 (A2 PCB) has failed. Replace the A2 PCB and recalibrate the LO2 as described in Chapter 6.

RF Unleveled

This problem is usually caused by setting the Source power above the instrument capabilities for the frequency range selected. If the Source power is set above default value (0 dB) and reducing the source power causes the message to disappear, the 37XXXD is not malfunctioning.

If the message appears and the Source power is at default power or lower, the 37XXXD is not operating correctly. Performing the Source ALC Calibrations (Chapter 6) may solve the problem. If the problem persists, the difficult nature of this problem means the best solution is to return the VNA to an Anritsu Service Center for repair.

IF Cal Failures (during self-test or measurement)

If only "Test A" is noted on the front panel error message(s) or **<OVL>** is present in the Service Log only in the "A" voltages section, the problem is most likely a fault of the A3 PCB.

If only "Test B" is noted on the front panel error message(s) or **<OVL>** is present in the Service Log only in the "B" voltages section, the problem is most likely a fault of the A6 PCB.

If only "Ref" is noted on the front panel error message(s) or **<OVL>** is present in the Service Log only in the "R" voltages section, the problem is most likely a fault of the A4 PCB.

If there are multiple (usually 3) "IF Cal Failure" error messages on the 37XXXD front panel or **<OVL>** appears in the "A," "B," and "R" voltages sections of the Service Log, the problem is most likely a failure of the 10 MHz internal time base. Replace the A7 PCB.

7-8 MEASUREMENT ACCURACY PROBLEMS

All Data on All Channels is Greatly Inaccurate

Refer to the block diagrams in Chapter 3 that are labeled "Signal Paths."

For 50 and 65 GHz models, refer to the block diagram of the Test Signal paths (Figure 7-4). Also, refer to Tables 7-2 through 7-4. Use of a spectrum analyzer, oscilloscope, and DVM will be useful to find the defective assembly.

The instrument may be in an unusual setup, such as a non-phase-locked “Receiver” mode, or the internal memory buffers may have corrupt data due to a process that was started, but incorrectly terminated. To correct this problem, press the **Default Program** key, then the 0 key to return the instrument to normal measurement condition and clear the memory buffers. Reload all of the coefficient disks from the Calibration Kits.

Excessive Ripple in the Display of Low-Loss Devices

Ensure that all of the calibration coefficients are loaded into the VNA. The coefficients may have been erased by a **Default Program** / 0 reset.

The calibration selected should be 12 Term. Also perform the calibration using sliding terminations rather than broadband fixed terminations.

Insufficient System Dynamic Range

Select “Include Isolation” and increase the RF Source power during the calibration setup.

Before measuring the Isolation Devices during the calibration, press the Video IFBW key and select “10 Hz Minimum”.

During the measurement of the DUT, select “10 Hz IF Bandwidth.”

Perform the automated “System Dynamic Range” test found in the 3700Test Program (described in Chapter 4). If this test fails, the problem is typically solved by replacement of the Sampler/Down Conversion Module.

7-9 NON-RESPONSE OR OTHER UNUSUAL BEHAVIOR

Many problems may be solved simply by performing a Master Reset, which clears all memory buffers and sets the instrument to factory-default settings. To do this, press the Default Program key, then the 0 key. Note that this will also clear all setup memories (#1 through #10), and will delete all Cal Kit coefficients. Cal Kit coefficients must be reloaded using the floppy disk from the Cal Kit.

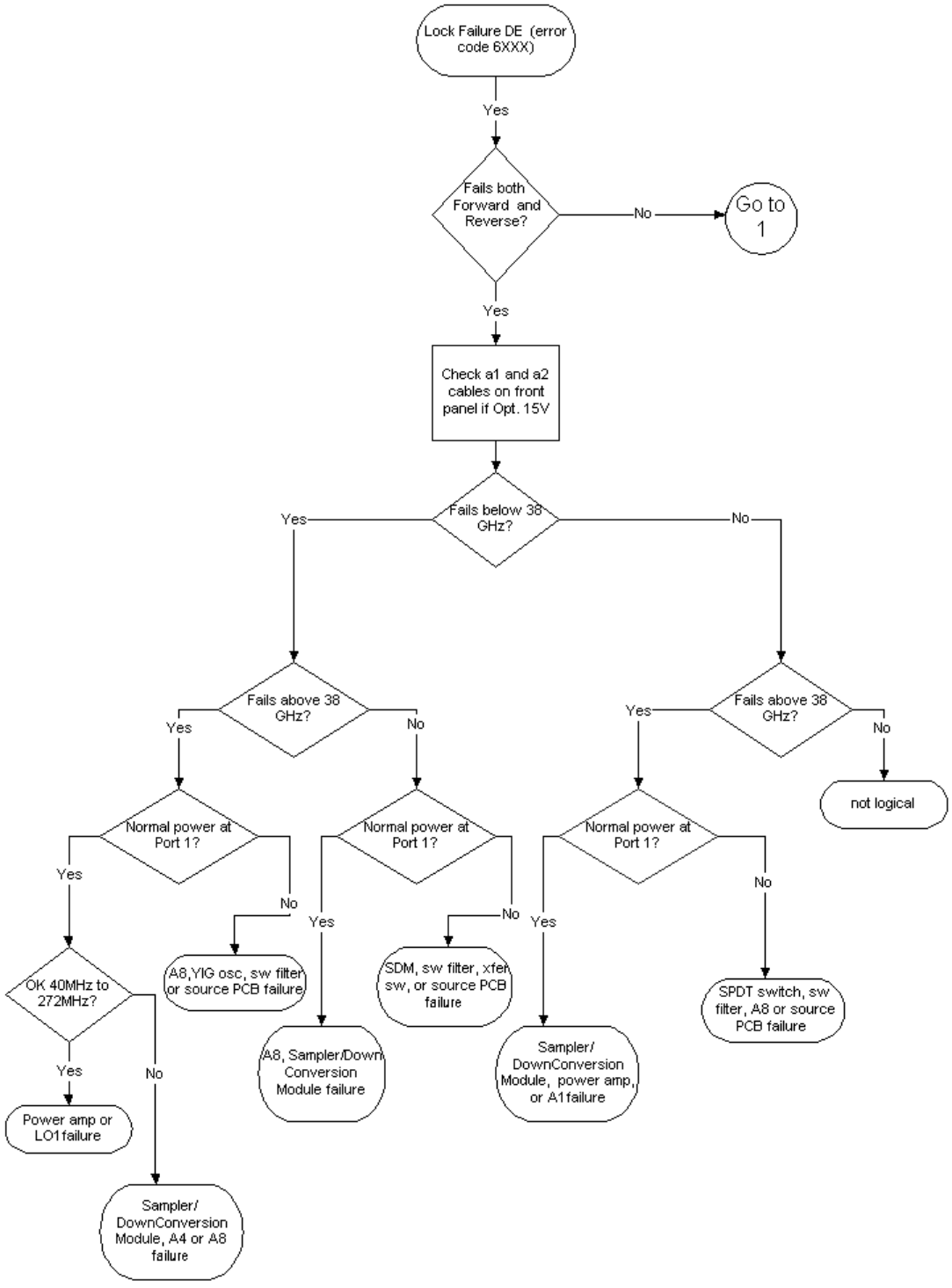


Figure 7-2. *Error Code DE Lock Failure Troubleshooting (50 and 65 GHz models only) (1 of 3)*

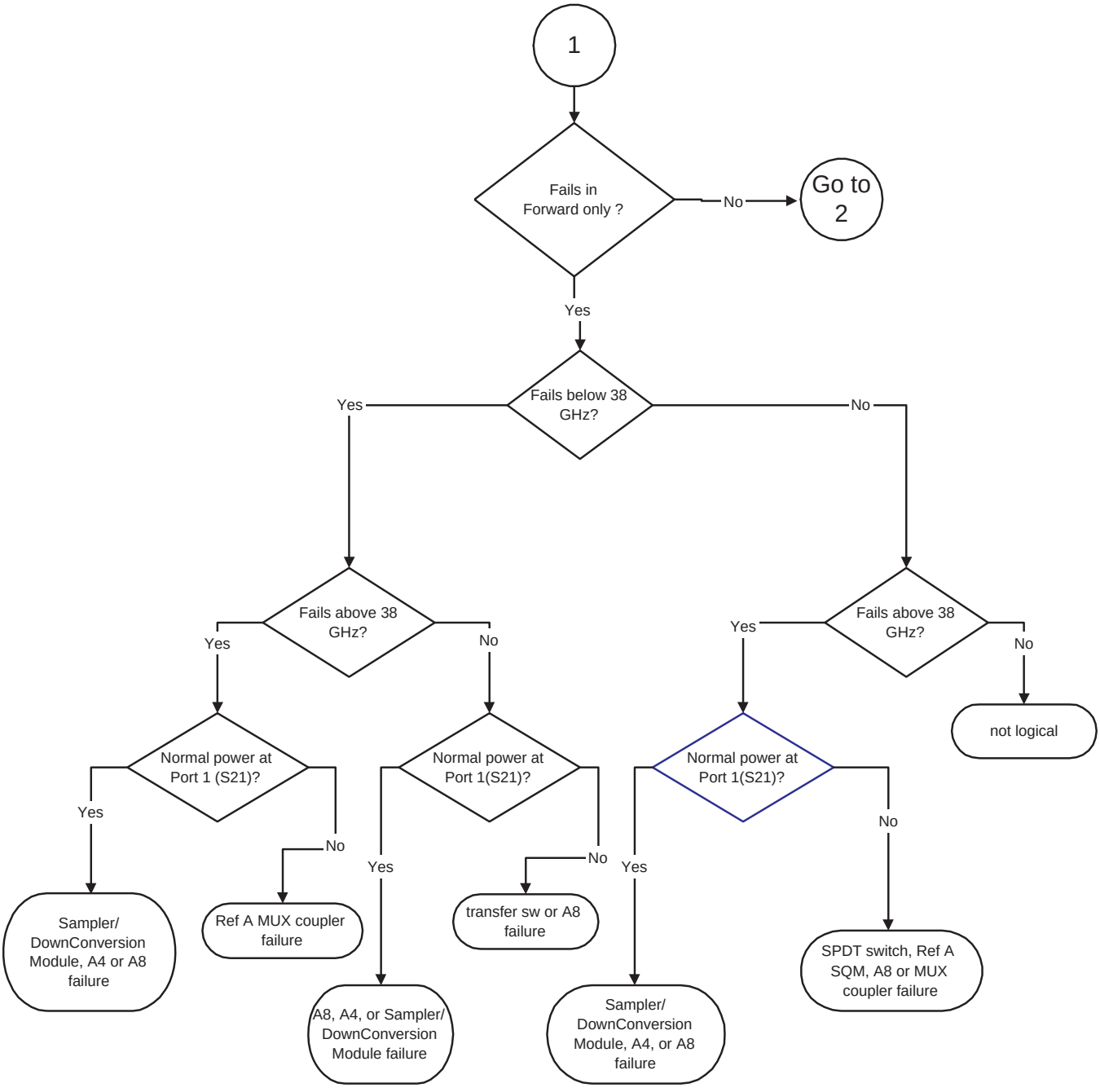


Figure 7-2. *Error Code DE Lock Failure Troubleshooting (50 and 65 GHz models only) (2 of 3)*

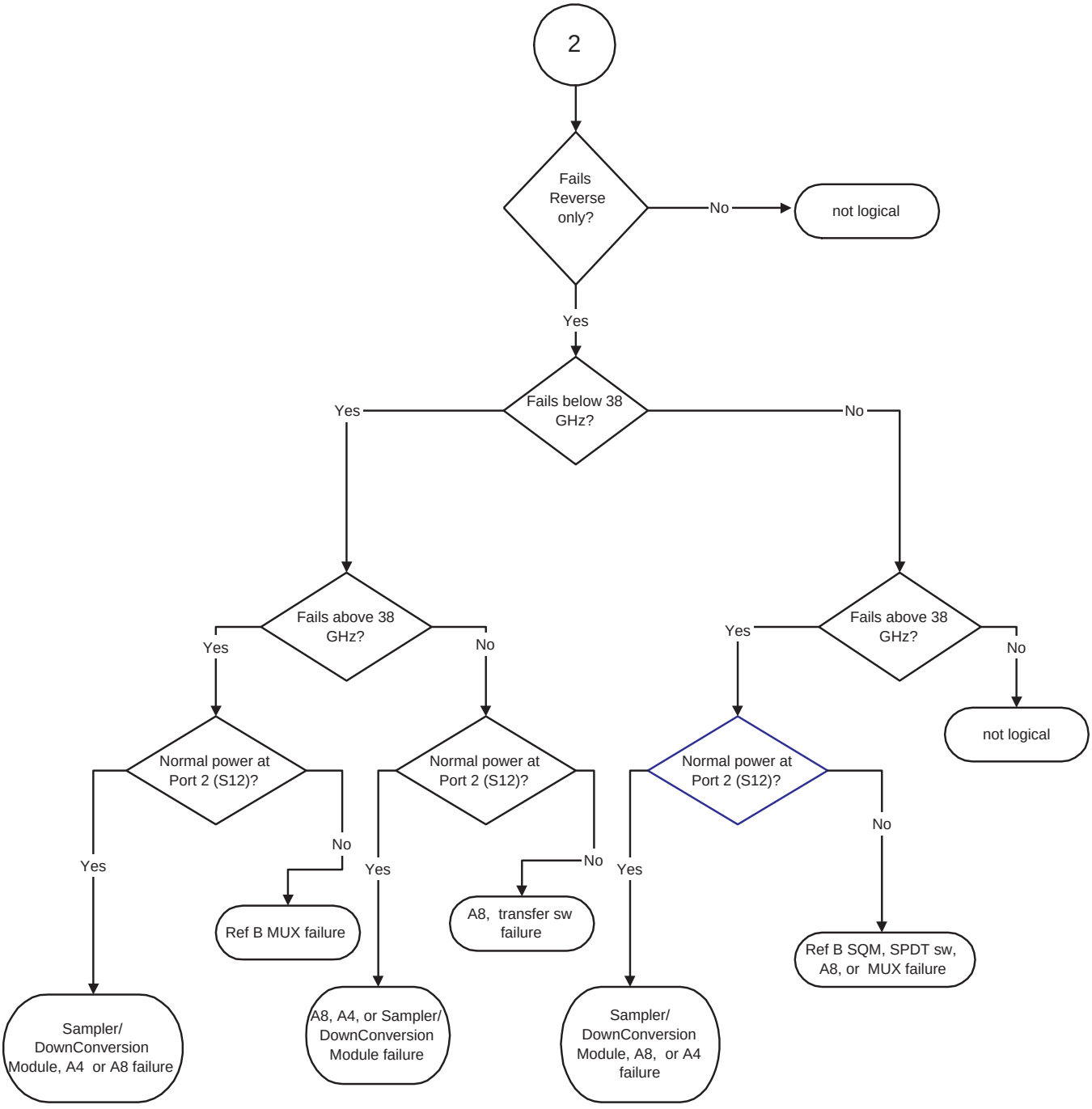


Figure 7-2. *Error Code DE Lock Failure Troubleshooting (50 and 65 GHz models only) (3 of 3)*

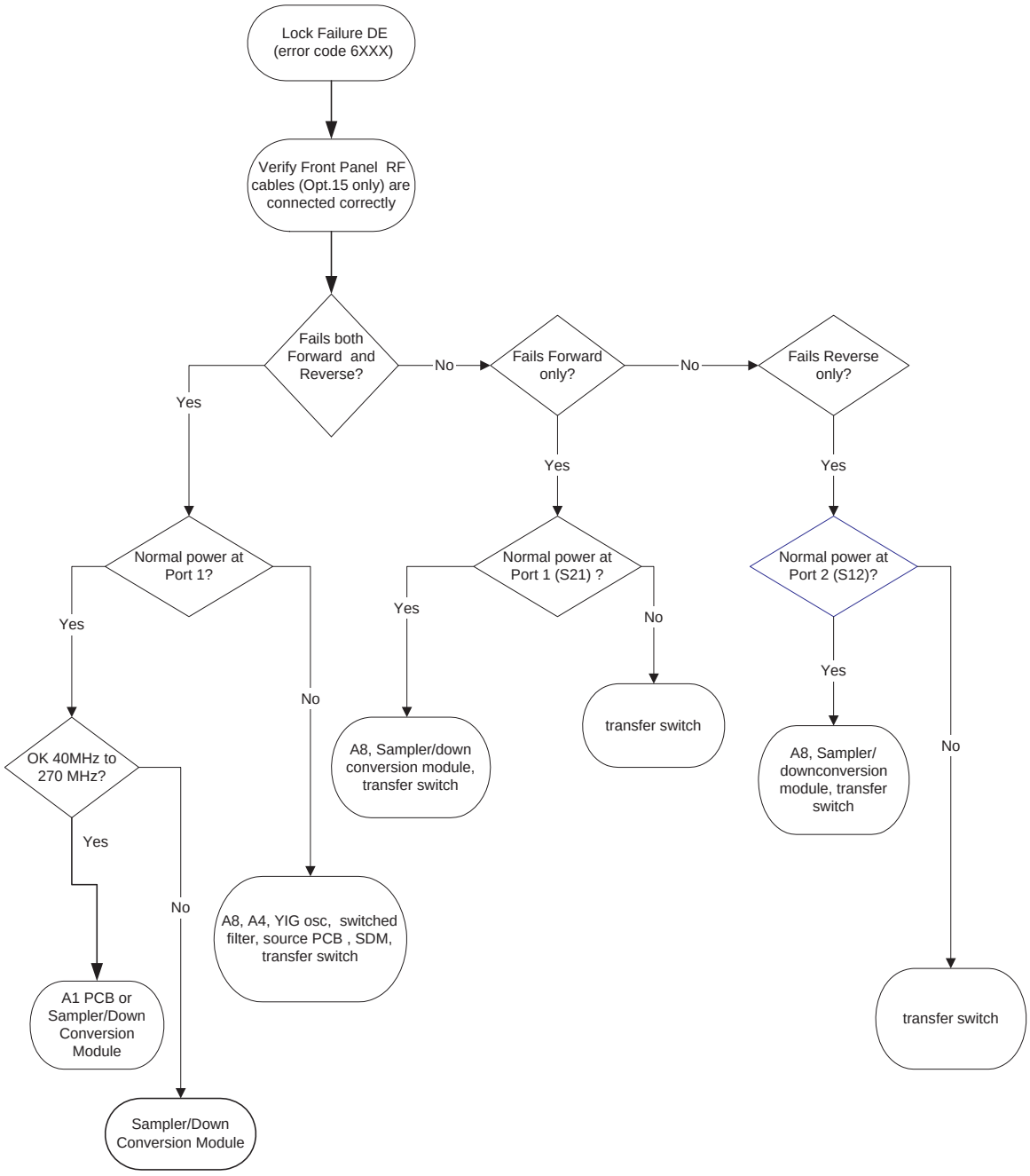


Figure 7-3. *Error Code DE Lock Failure Troubleshooting (20 GHz and 40 GHz models only) (1 of 1)*

Table 7-2. *Typical Reference Signal Values in dBm (50 and 65 GHz models only)*

Frequency	SQM In	SDM Out	MUX J4	MUX J1	Sampler/Down Conversion Module Input
20 GHz	NA	+18	+6	NA	–26
37 GHz	NA	+20	+4	NA	–28
40 GHz	+19	NA	NA	+14	–28
50 GHz	+18	NA	NA	+14	–23
65 GHz	+16	NA	NA	+10	–26

Table 7-3. *Typical Transfer Switch (D27030) Voltages (CW, Single Channel Display, 50 GHz and above models only)*

Wire Color	Below 38 GHz		Above 38 GHz	
	S21	S12	S21	S12
Brown	+2.0	–3.3	+2.0	+2.0
Black	–6.7	+1.6	+1.6	+1.6
White	+1.6	–6.8	+1.6	+1.6
Grey	–3.3	+2.0	+2.0	+2.0

Table 7-4. *Typical SPDT Switch (part number 29855) Voltages (CW, Single Channel Display, 50 GHz and above model only)*

Wire Color	Forward	Reverse
Brown	+1.2	–3.7
Grey	–3.7	+1.2

Chapter 8
Removal and Replacement Procedures

Table of Contents

Chapter 8
Removal and Replacement Procedures

8-1 INTRODUCTION

This chapter provides procedures for removing and replacing the 37XXXD field exchangeable assemblies and components. When using these procedures, please observe the warning and caution notices below:

> ***WARNING***
>
> Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels.

> ***CAUTIONS***
>
> Many assemblies in the VNA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. *Always* observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.
>
> 37XXXD instruments are covered by a three year factory warranty. Unauthorized repair attempts by non-Anritsu service personnel will void this warranty.
>
> All RF connections (at the Wxxx cables) should be torqued to 8 in/lbs using the 01-201 wrench from a Calibration Kit. Check for RF discontinuities and other failures using the first six to eight tests in the 2300-178 program.

8-2 EQUIPMENT REQUIRED

All procedures in this chapter require the use of either a #1 or #2 size Phillips type screw driver. Most procedures require the use of a 5/16 inch wrench and the Anritsu 01-201 (8 inch/pounds) Torque Wrench.

8-3 COVERS

Adjustment and troubleshooting operations require removal of the top cover. Replacement of some VNA assemblies and parts require removal of all covers. The following procedures describe this process.

> ***NOTE***
> It is only necessary to loosen the VNA handle assemblies to remove the top, bottom, or side covers. However, if the front panel is to be removed, remove the handle assemblies at this time.

Preliminary:

- ❑ Switch the VNA power **off** and remove the power cord.

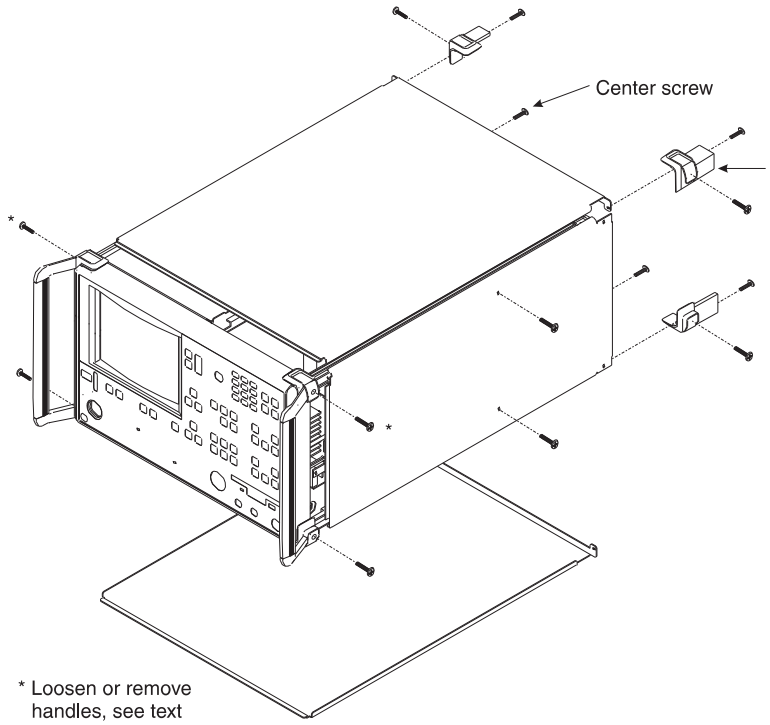


Figure 8-1. *Exploded View of 37XXXD Chassis Covers*

Procedure:

Step 1. Loosen (or remove) the right and left handle assemblies, as follows:

- ■ Place the VNA on its top (bottom-side up).
- ■ Loosen/remove the screws at the sides of the handle assemblies.
- ■ If removing handles, pull them away from unit and set aside.

> ***CAUTION***
>
> The green headed screws have Metric threads.

Step 2. To remove the top cover:

- Place the VNA in normal (top-side up) position.
- Remove the feet from the two top corners at the rear of the VNA (Figure 8-1).
- Remove the center screw from the rear of the top cover.
- Lift and slide the top cover away from the VNA.

Step 3. To remove the bottom cover:

- Place the VNA on its top (bottom-side up).
- Remove the feet from the two bottom corners at the rear of the VNA.
- Remove the center screw from the rear of the bottom cover.
- Lift and slide the top cover away from the VNA.

Step 4. To remove the left cover:

- Place the VNA on its right side (monitor down).
- If not already done, remove the feet from the two left-side corners at the rear of the VNA.
- Remove two center screws from the left cover.
- Remove the center screw from rear of the left side cover.
- Lift and slide the side cover away from the VNA.

Step 5. To remove the right cover:

- Place the VNA its left side (monitor up).
- If not already done, remove the feet from the two right-side corners at the rear of the VNA.
- Remove the center screw from the rear of the right side cover.
- Remove the center screw from the rear of the right side cover.
- Lift and slide the side cover away from the VNA.

To replace the instrument covers, perform the steps above in the reverse order.

8-4 A1 TO A16 PCBS

This section provides instructions for removing and replacing the A1 through A9 and A13 through A16 PCBs, which are located underneath the covers of the large and small card-cages, respectively.

Preliminary:

- ❑ Switch the VNA power to **off**. Remove the power cord.
- ❑ Remove the top cover (Section 8-3).

A1 to A16 PCBs

Procedure:

Step 1. Place the VNA in normal (top-side up) position.

Step 2. Remove the two screws that secure the large card-cage cover (Figure 8-2).

Step 3. Remove the two aluminum card-cage covers and set them aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight up.

To replace the PCB(s) and covers, perform the steps above in the reverse order.

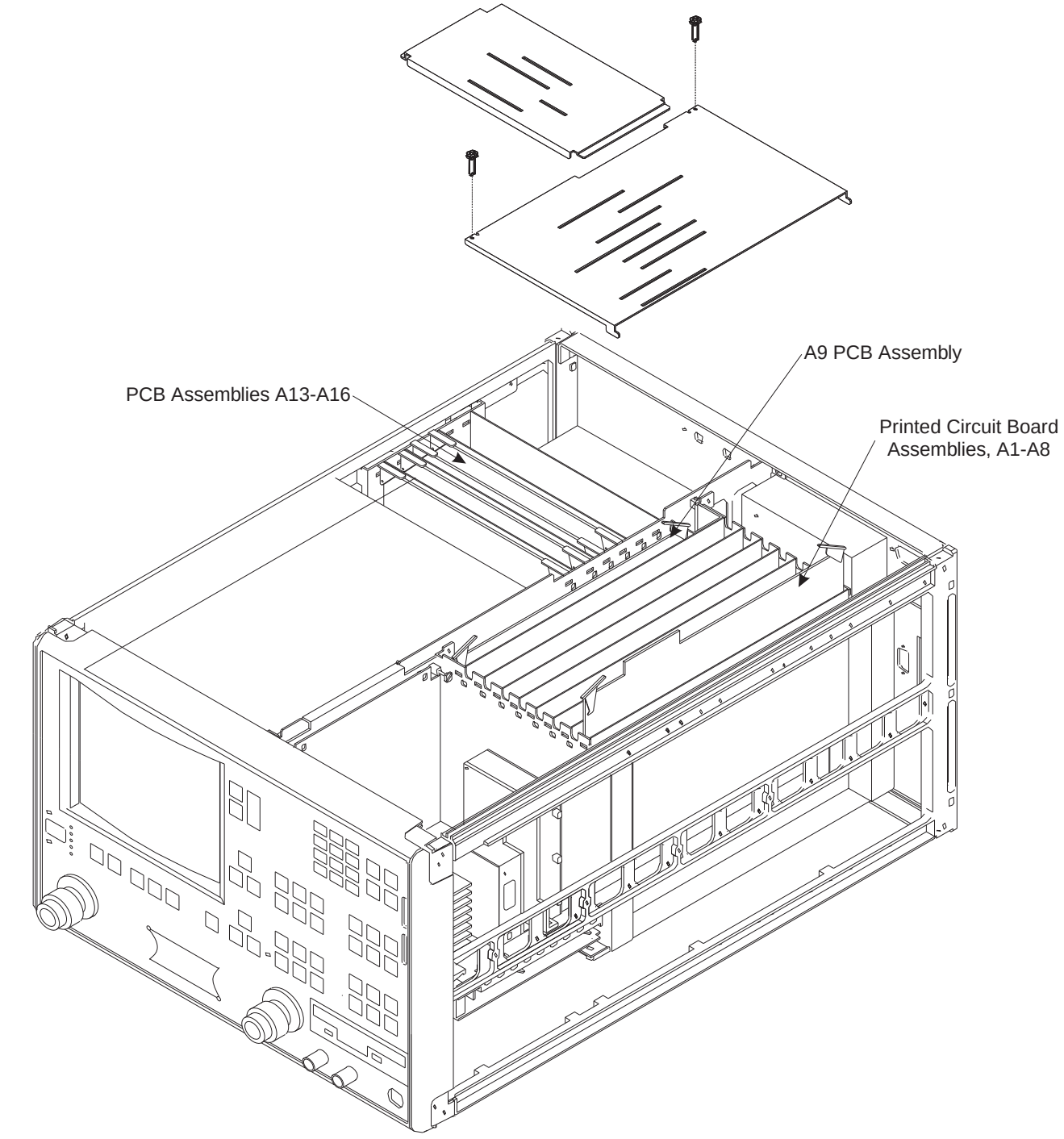


Figure 8-2. *A1 to A16 PCB Assemblies Removal Diagram*

8-5 A24 VME BUS TERMINATOR PCB

This section provides instructions for removing and replacing the A24 VME Bus Terminator PCB assembly.

Preliminary:

- ❑ Switch VNA power **off**. Remove the power cord.
- ❑ Remove bottom cover (Section 8-3).

Remove/Replace Procedure:

Step 1. Place the VNA on its top (bottom-side up).

Step 2. Locate the A24 PCB assembly (Figure 8-3). Unplug A24 PCB assembly from the A17 Motherboard PCB by gently pulling straight up on each side.

> ***CAUTION***
>
> Be careful not bend or disturb the hard coax lines located near the right edge of the A24 PCB.

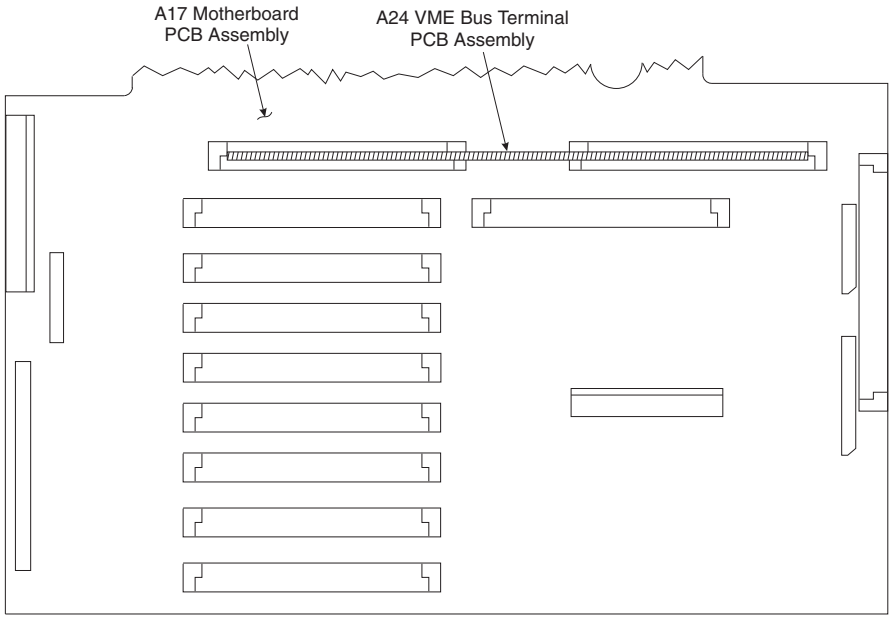


Figure 8-3. *Location of the A24 VME Bus Terminator PCB Assembly*

8-6 FRONT PANEL ASSEMBLY

This section provides instructions for removing and replacing the VNA Front Panel assembly.

Equipment Required:

- Open-end wrench, 1 inch
- Hex driver, 3/32 inch, ball end

Preliminary:

- Switch the VNA power to **off** and remove the power cord.
- Remove the handle assembles and all covers (Section 8-3).

> ***NOTES***
>
> It is not necessary to remove the front panel assembly to replace the floppy disk drive. To replace a coupler or the floppy drive, refer to Section 8-8.
>
> On instruments with Option 15V (found only on 50 and 65 GHz instruments), there is a very high risk of damage to RF cables and connectors during re-assembly. Such instruments should be returned to an Anritsu Service Center for repairs to the front panel assembly.

Remove/Replace Procedure:

Step 1. Place the VNA in normal (top-side up) position.

Step 2. Remove the four corner screws and the top center screw that secure the front panel assembly to the chassis (see Figure 8-5).

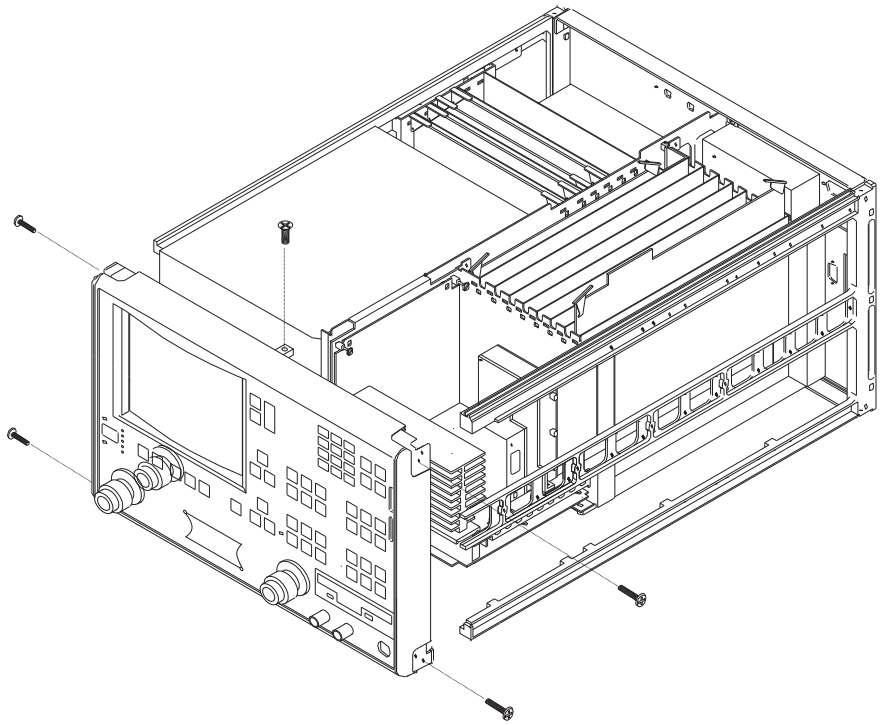


Figure 8-5. *Removal of Front Panel Assembly*

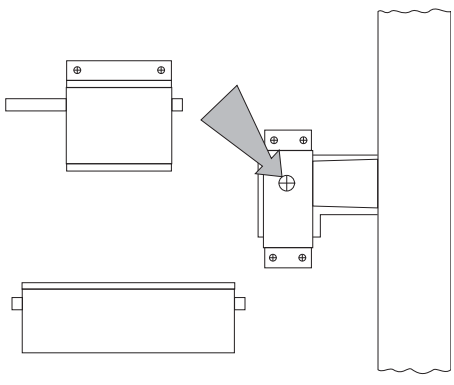


Figure 8-4. *Removal of Test Set Module*

Step 3. Place the VNA on its top (bottom-side up).

Step 4. Remove the screw that fastens the front panel casting extension lip to the Test Set Module tray. (See diagram at left.)

Step 5. Using a 1 inch open-end wrench, remove the nuts and washers that secure the Port 1 and Port 2 couplers/bridges to the front panel casting.

Step 6. Disconnect the cable from the front panel Power switch to the power supply control PCB.

Step 7. Disconnect the cable from the front panel Keyboard interface connector to connector J16 on the A17 Motherboard PCB.

Step 8. Disconnect all RF cables that are connected between the RF Deck and the front panel.

Step 9. On 300 series models, disconnect the cables from the front panel Bias Input BNC connectors to connector P2 on the A18 Rear Panel PCB at A18, P2 end. (A18, P2 is the connector nearest to the bottom lip of the rear panel.)

Step 10. On 50 GHz and 65 GHz models, remove the three hex head screws that attach each coupler to the front panel.

Step 11. Pull the front panel assembly several inches away from chassis.

Step 12. Disconnect the cable from the A17 Motherboard PCB to connector J1 on the A20 Front Panel PCB.

Step 13. Pull the front panel assembly free and set it aside.

To replace the front panel assembly, perform the steps above in the reverse order.

8-7 LIQUID CRYSTAL DISPLAY (LCD)

This section provides instructions for removing and replacing the internal LCD assembly. This LCD display needs no periodic maintenance. Its life is estimated to be 50,000 hours by the manufacturer. If the A15 PCB and the backlight driver PCB have been determined to be functioning correctly, replacing the LCD will likely solve display problems.

> ***CAUTION***
> Due to the likelihood of damage to RF cables and connectors, Anritsu advises to NOT remove the front panel of 50 and 65 GHz instruments having Option 15V to perform this repair.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove the right handle, top and bottom covers, and right side cover (Section 8-3).

Remove/Replace Procedure:

The LCD and shield is held in place by 4 retaining screws that are clearly visible, but difficult to access.

The most appropriate procedure to replace the LCD will depend on the presence or absence of Option 15 (front panel RF access cables).

When Option 15 is installed, the front panel should not be removed. In this case, remove the Source Module and the Power Supply to access the 4 LCD retaining screws.

When Option 15 is not installed, removing the front panel is the easier method of accessing the LCD.

Removing the Power Supply is described in Section 8-11; removing the Source Module is described in Section 8-14; removing the Front Panel is described in Section 8-6.

Install the new display by reversing the above procedures.

> ***NOTE***
> All RF connections (at the Wxxx cables) should be torqued to 8 in/lbs using the 01-201 wrench from a Calibration Kit. Check for RF discontinuities and other failures using the first six to eight tests in the 2300-178 program.

8-8 FLOPPY DISK DRIVE

Replacement instructions are included with the replacement floppy disk drive. Do NOT remove the front panel to replace the floppy disk drive.

8-9 REAR PANEL ASSEMBLY

This section provides instructions for removing and replacing the Rear Panel Assembly.

Equipment Required:

- ❑ Phillips Screwdriver (#2)
- ❑ Open-end Wrenches (various sizes)

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).

> ***NOTE***
> It is not necessary to remove the rear panel to remove the A18 rear panel PCB.

Remove/Replace Procedure:

Step 1. Disconnect all cables which are connected to the rear panel and to the A18 rear panel PCB.

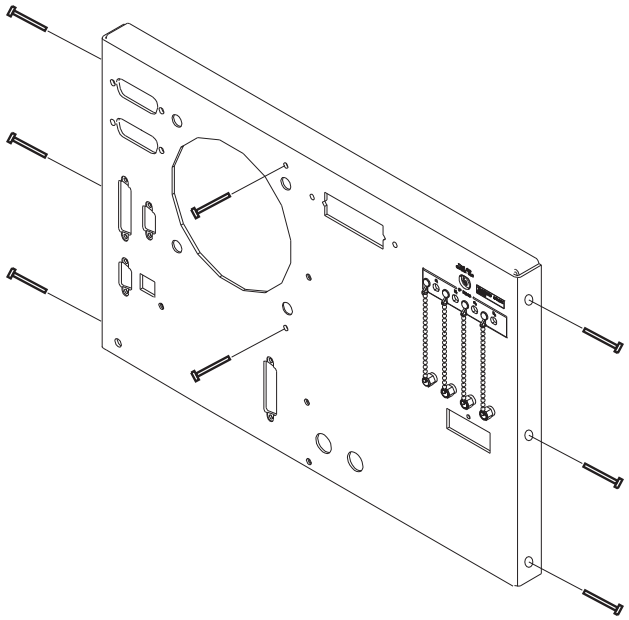


Figure 8-6. *Rear Panel Mounting Screws*

Step 2. Remove the three screws on each side of the chassis that fasten to the rear panel assembly.

Step 3. Remove the two screws located near top and middle of rear panel (near fan-mounting screws).

To replace the Rear Panel Assembly, perform the steps above in the reverse order.

8-10 FAN ASSEMBLY

This section provides instructions for removing and replacing the Rear Panel Fan Assembly.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).
- ❑ Remove the Rear Panel (Section 8-9).

Remove/Replace Procedure:

Step 1. Place the Rear Panel Assembly on the work surface with the A18 Rear Panel PCB up.

Step 2. Disconnect the two conductor fan power cable at connector P6 of the A18 PCB.

Step 3. Turn the Rear Panel Assembly over, and remove the four screws that fasten the fan guard and fan assembly to the rear panel.

Step 4. Remove the fan guard and separate the fan from the rear panel.

To replace the Rear Panel Fan Assembly, perform the steps above in the reverse order.

8-11 POWER SUPPLY MODULE

This section describes removing and replacing the Power Supply module that is mounted on the frame of the instrument behind the LCD.

Power Supply Removal:

> ***DANGER***
> Failure to remove the power cord before beginning this operation can result in a fatal electric shock.

Step 1. Remove the power cord from the instrument.

Step 2. Remove the 37000 top cover, bottom cover, and left side cover.

Step 3. Unplug the large power supply cables from J4 and J13 on the 37000 motherboard.

Step 4. At the small daughter board of the power supply, unplug the power switch wire connector (black and white twisted pair).

Step 5. Remove the power supply from the 37000 frame by removing the 6 screws that fit through the left side of the frame.

Step 6. Tilt up the front end of the supply so that you can see the clear plastic cover over the Line Voltage wires.

Step 7. Remove the screws holding the clear cover, remove the cover and disconnect the wires.

Step 8. Remove the power supply.

Power Supply Installation:

Step 1. Attach the Line Voltage wires to the terminals as shown in Figure 8-7.

Step 2. Reinstall the clear safety cover over the Line Voltage wires.

Step 3. Reinstall the supply by performing the opposite of the removal instructions.

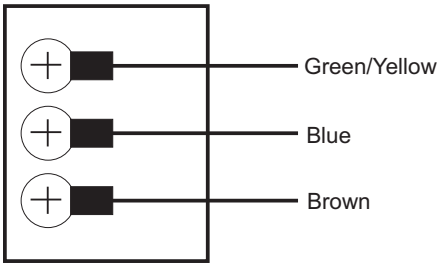


Figure 8-7. *Power Supply Voltage Wire Connections*

8-12 A18 REAR PANEL PCB

This section provides instructions for removing and replacing the A18 Rear Panel PCB assembly.

Equipment Required:

- ❑ Nut Driver, 9/32 inch
- ❑ Nut Driver, 3/16 inch
- ❑ Phillips Screwdriver (#2)

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).

Remove/Replace Procedure:

Step 1. Disconnect all cables that are connected to the A18 PCB.

Step 2. Remove all eight 3/16 inch nuts that hold the various rear panel connectors.

Step 3. Remove all four 9/32 inch nuts holding the GPIB connectors.

Step 4. Remove the Phillips screw located next to the rear panel warning label (lower left corner).

Step 5. Remove the A18 PCB.

To replace the A18 Rear Panel PCB assembly, perform the steps above in the reverse order.

8-13 TEST SET MODULE ASSEMBLIES

Replacement of any item on the Test Set Module will require that all Source Calibrations and the Source Lock Threshold Calibration be performed (see Chapter 6). Performing all of the tests in the 3700Test program (Section 4-4) is also strongly suggested.

Equipment Required:

- ❑ Connector torque wrench (5⁄16 inch), Anritsu Model 01-201, or equivalent
- ❑ 1 inch open-end wrench and 3⁄32 inch ball end hex wrench (only if couplers are to be replaced)

> ***CAUTION***
>
> Throughout these procedures, *always* use the 5⁄16 inch connector torque wrench for connecting the Test Set Module semi-rigid coaxial lines and RF/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

Preliminary:

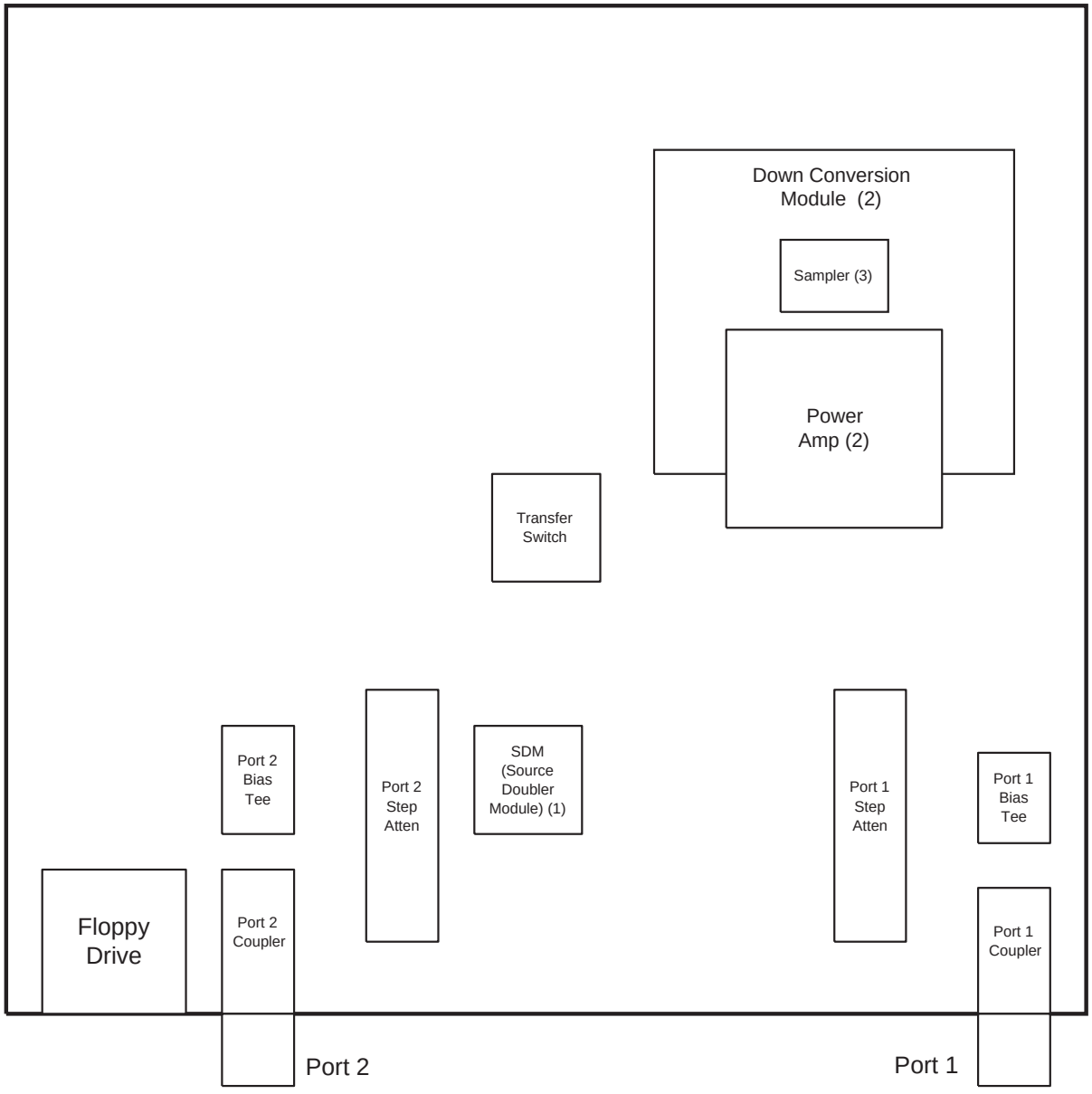
- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).

Remove/Replace Procedure:

All RF components found on the Test Set Module may be removed and replaced simply by removal of the associated RF cabling, Phillips-head screws, and unplugging bias cables. Replacement parts supplied by Anritsu have instructions where instructions are necessary.

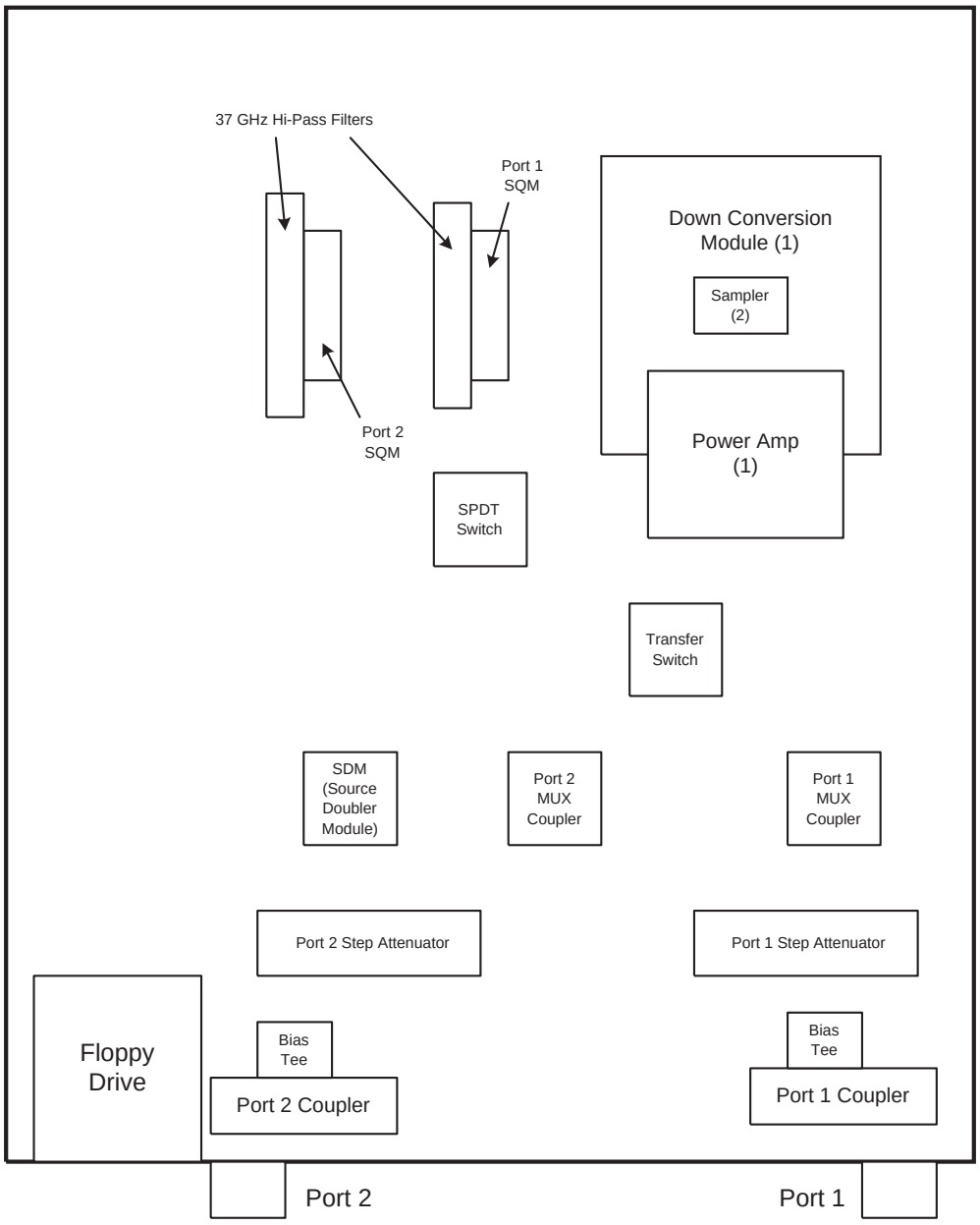
Take careful note of all warnings and notes printed on the first page of this Chapter. RF connectors are easily damaged. RF cable connections that are improperly mated will cause discontinuities resulting in measurement errors.

Figures 8-8 and 8-9 show the locations of all RF components located on the Test Set assembly.



Notes:
1. SDM's are present only on 40 GHz and above models.
2. The Down Conversion Module and Power Amp must be replaced only as a matched set.
3. Do not disconnect the sampler from the Down Conversion Module.

Figure 8-8. *Test Set Module Components Layout Diagram for non 50 and 65 GHz Models*



Notes:
1. The Down Conversion Module and Power Amp must be replaced as a set.
2. Do not disconnect the sampler from the Down Conversion Module.

Figure 8-9. *Test Set Module Components Layout Diagram for 50 and 65 GHz Models*

8-14 SIGNAL SOURCE MODULES

The following sections provide instructions for removing the signal Source Module for replacement of individual components. (See the next section for removal of the A21A2 PCB without removing the entire Source Module assembly.) Removal of individual Source components is covered in the next sections

> ***NOTE***
> After replacement of any itme in the Source Module, all Source calinrations (frequency, ALC, Source Lock Threshold) nust be performed. See Chapter 6.

Equipment Required:

- ❑ Connector torque wrench ($^{5}/_{16}$ inch), Anritsu Model 01-201, or equivalent.

> ***CAUTION***
> Throughout these procedures, *always* use the $^{5}/_{16}$ inch connector torque wrench for connecting the Signal Source Module semi-rigid coaxial lines and RF/microwave components. Use of improper tools may damage the connectors, resulting in degraded instrument performance.

Preliminary:

- ❑ Switch the VNA power to **off** and remove the power cord.
- ❑ Remove all covers (Section 8-3).

Removal of Signal Source Module

Use the following procedure to remove the Signal Source Module from the chassis. This step is necessary before any of the module components can be removed/replaced.

Procedure:

Step 1. Turn the instrument upside down and remove the RF cable(s) that pass through the holes drilled in the motherboard (identified as W81, W87, W179, and W180 on different models).

Step 2. Return the instrument to the normal operating position and, using steps below, remove the Source Module.

Step 3. Disconnect the two cables from the A21A2 PCB.

Step 4. Loosen the two captivated metal screws that attach the A21A2 bracket to the instrument frame.

Step 5. Disconnect the ribbon cable from the Down Conversion Module.

Step 6. Remove the cables W347, W235 and the fixed attenuator between them (found on the right side of the Source Module).

Step 7. Remove the three screws on the right side of the instrument frame from the Source Module frame.

Step 8. Lift the Source Module up, and remove by tipping the top to the right to clear the instrument frame.

To replace the Signal Source Module, perform the steps above in the reverse order.

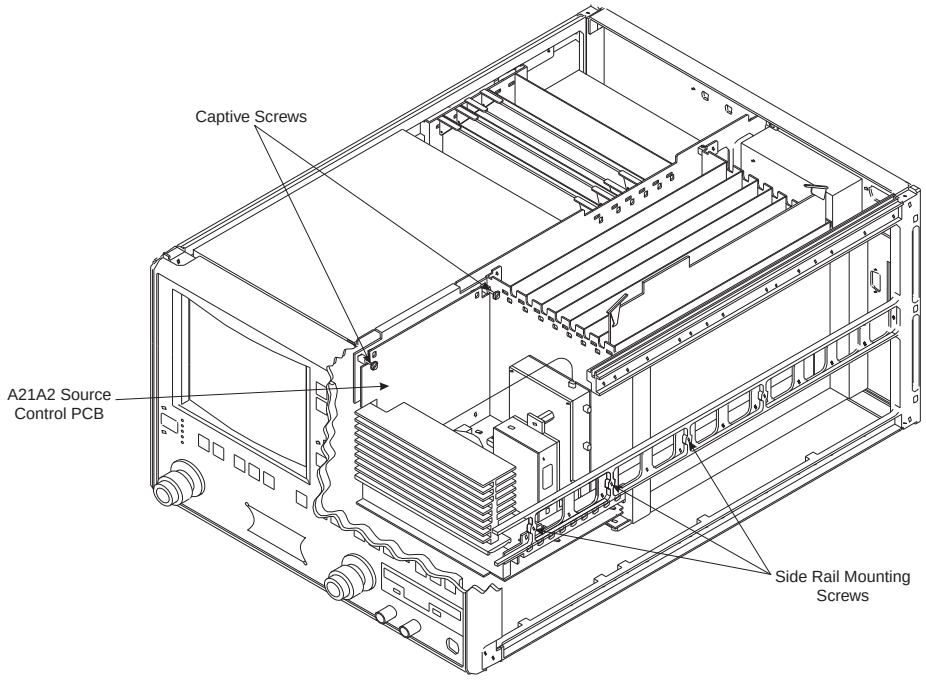


Figure 8-10. *Signal Source Module Removal Details*

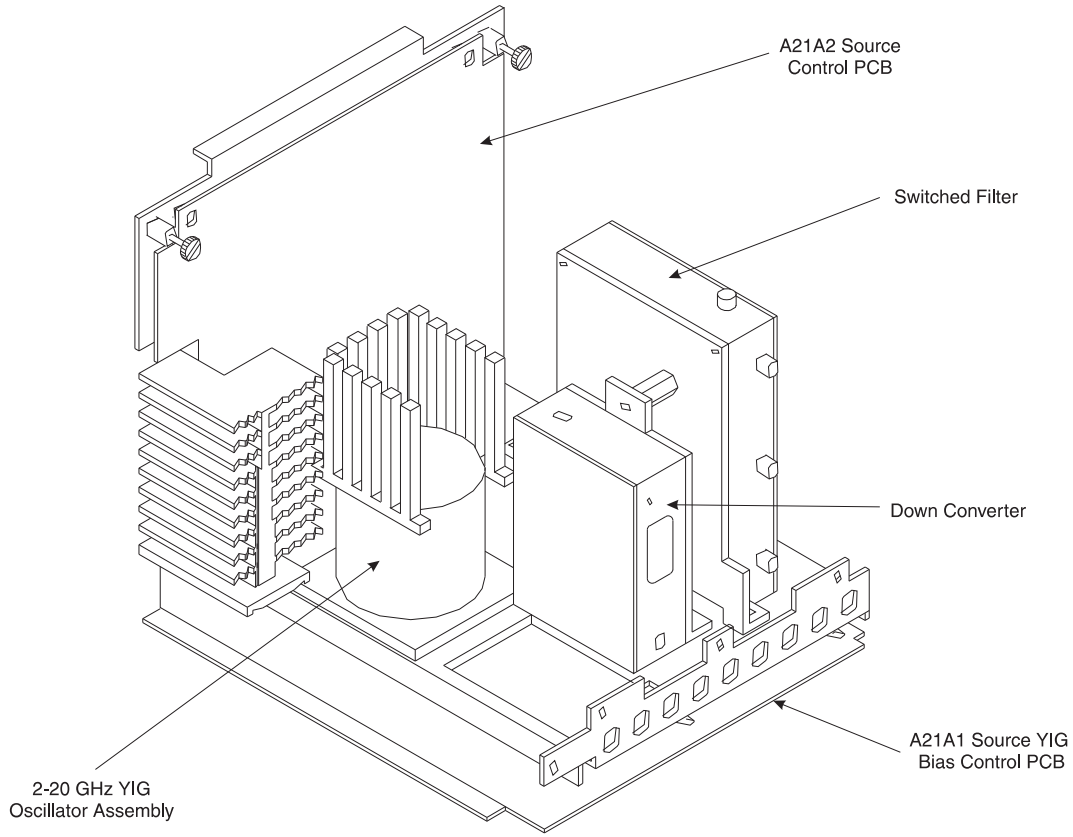


Figure 8-11. *Signal Source Module Assemblies Removal Details*

A21A2 Source Control PCB

Use the following procedure to remove/replace the A21A2 Source Control PCB assembly.

Procedure:

Step 1. Unfasten two black plastic PCB retainers at the top corners of the A21A2 Source Control PCB. To unfasten, turn screwdriver slot ¼ turn *counter-clockwise*.

Step 2. Pull the top of the A21A2 PCB away from the source module chassis back plate to clear PCB retainers. Gently pull up to disconnect the A21A2 PCB from the socket on the A21A1 Source YIG Bias Control PC. Remove from Source Module.

To replace the A21A2 Source Control PCB assembly, perform the steps above in the reverse order.

A21A1 Source YIG Bias Control PCB

Use the following procedure to remove/replace the A21A1 Source YIG Bias Control PCB assembly.

Procedure:

Step 1. Remove the Source Module as described in the beginning of this section.

Step 2. Disconnect the Switched Filter assembly power cable from connector J1 of the A21A1 Source YIG Bias Control PCB. (Pull up gently on ribbon cable to disconnect.)

Step 3. Similarly, disconnect the Down Converter assembly power cable from connector J4 of the A21A1 PCB.

Step 4. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector handle to disconnect.

Step 5. Remove the screw that fastens the front apron of the source module chassis to the heatsink of the A21A1 PCB. See Figure 8-11.

Step 6. Remove the four screws that fastens the back plate of the source module chassis to the heatsink of the A21A1 PCB.

Step 7. Place the Signal Source Module on its‘ back plate.

Step 8. Unfasten the six PCB retainers on the bottom of the A21A1 PCB. (To unfasten, turn screwdriver slot ¼ turn *counter-clockwise*.) Gently separate the A21A1 PCB (including the heat sink) from the Signal Source Module.

To replace the A21A1 Source YIG Bias Control PCB assembly, perform the steps above in the reverse order.

Switched Filter Assembly

Use the following procedure to remove/replace the Switched Filter assembly.

Procedure:

Step 1. Disconnect the power cable from connector P1 at the rear of the Switched Filter assembly. (Use a small screw driver to pry up gently at each end of the connector, as necessary.)

Step 2. Disconnect the semi-rigid coaxial lines from connector J6 (top) and connector J3 (lower-front) of the Switched Filter assembly.

Step 3. Disconnect the semi-rigid coaxial line from the RF INPUT (top) connector of the *Down Converter* assembly.

Step 4. Remove the two screws that fasten the Switched Filter assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 5. Disconnect the semi-rigid coaxial line from connector J1 (bottom) of the Switched Filter assembly. Put this coaxial line aside for re-use.

> ***NOTE***
> When replacing the Switched Filter assembly, connect the semi-rigid coaxial line to the bottom connector (J1), before attaching the assembly to the Signal Source Module.

To replace the Switched Filter assembly, perform the steps above in the reverse order.

Down Converter Assembly

Use the following procedure to remove/replace the Down Converter assembly.

Procedure:

Step 1. Disconnect the power cable from connector P1 at the front of the Down Converter assembly.

Step 2. Disconnect the semi-rigid coaxial lines from the RF INPUT connector and RF OUTPUT connector of the Down Converter assembly.

Step 3. Remove the two screws that fasten the Down Converter assembly to the source module chassis and lift the assembly from the Signal Source Module.

To replace the Down Converter assembly, perform the steps above in the reverse order.

YIG Oscillator Assembly

Use the following procedure to remove/replace the YIG Oscillator assembly.

Procedure:

Step 1. Disconnect the YIG Oscillator assembly power cable from connector J3 of the A21A1 PCB. Pull up on the flexible circuit connector handle to disconnect.

Step 2. Disconnect the semi-rigid coaxial line from the connector J6 (top) of the *Switched Filter* assembly.

Step 3. Remove the four screws that fasten the YIG Oscillator assembly to the source module chassis and lift the assembly from the Signal Source Module.

Step 4. Disconnect the semi-rigid coaxial line from the output connector of the YIG Oscillator assembly. Put this coaxial line aside for re-use.

> ***NOTE***
> When replacing the YIG Oscillator assembly, connect the semi-rigid coaxial line removed in Step 4 to the output connector of the YIG Oscillator before attaching it to the Signal Source Module.

To replace the YIG Oscillator assembly, perform the steps above in the reverse order.

Appendix A
Connector Care and Handling

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Appendix A
Connector Care and Handling

A-1 INTRODUCTION

This appendix provides general, precautionary information and instructions pertaining to precision connectors.

A-2 PRECAUTIONS

The following paragraphs are precautionary notes relating to maintenance considerations for precision connectors

Pin Depth Problems

Based on Anritsu precision components returned for repair, destructive pin depth of mating connectors is the major cause of failure in the field. When a precision component is mated with a connector having a destructive pin depth, damage will likely occur to the precision component's connector. A connector is considered to have destructive pin depth when the center pin is too long in respect to the connector's reference plane (Figure B-1).

Before mating an unknown or new device with your VNA Port connectors or calibration devices, always measure the pin depth of the device's connectors. Use a Anritsu Pin Depth Gauge, or equivalent, for these measurements (Figure B-2). Also, measure the connector pin-depth of a device when intermittent or degraded performance is suspected.

Gauging sets for measuring the pin-depth of precision connectors are available from your nearest Anritsu Service center, or from the factory. Instructions for measuring connector pin-depth are included with the gauging set(s).

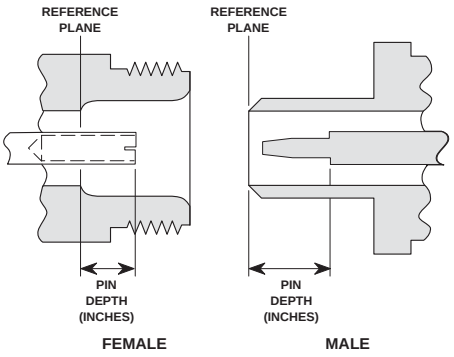

Figure A-1. *N Connector Pin Depth Definition*

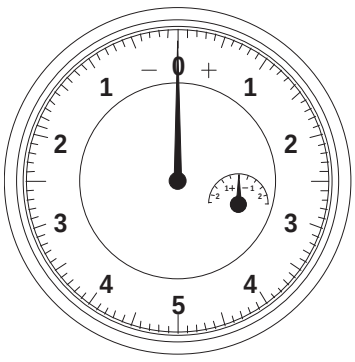

Figure A-2. *Pin Depth Gauge*

Pin-Depth Tolerance

The center pin of a precision connector has a tolerances measured in mils (one mil = 1/1000 inch). The connectors of test devices may not be precision types and they may not have the proper pin-depth. These connectors should be measured before mating to ensure suitability.

When gauging pin depth, if the connector being measured indicates out of tolerance in the "+" region of the gauge (Table B-1), the center pin is too long. *Mating under this condition will likely damage the mating connector.* On the other hand, if the test device connector indicates out of tolerance in the "–" region, the center pin is too short. While this will not cause any damage, it will result in a poor connection and a consequent degradation in performance.

Table A-1. *Connector Pin-Depth Tolerance*

Port/ Conn. Type	Pin Depth (MILS)	Gauge Reading
GPC-7	+0.000 –0.003	Same As Pin Depth
N Male	207 –0.000 +0.004	207 +0.000 –0.004
N Female	207 –0.004 +0.000	Same As Pin Depth
3.5 mm Male, Female	–0.000 +0.002	
K Male, Female	+0.0000 –0.0035	
V Male	+0.000 to –0.001	
V Female	+0.000 to –0.001	

Avoid Over Torquing Connectors

Over-torquing connectors is destructive; it may damage the connector center pin. Finger-tight is usually sufficient, especially on Type N connectors. Should it be necessary to use a wrench to tighten SMA or WSMA connectors, use a torque wrench that breaks at 8 inch-pounds. As a general rule, *never use pliers* to tighten connectors.

Teflon Tuning Washers

The center conductor on many precision connectors contains a small teflon tuning washer located near the point of mating (interface). This washer compensates for minor impedance discontinuities at the interface. The washer's location is critical to the connector's performance. *Do not disturb it*.

Avoid Mechanical Shock

Precision connectors are designed to withstand years of normal bench handling. Do not drop or otherwise treat them roughly. They are laboratory-quality devices, and like other such devices, they require careful handling.

Keep Connectors Clean

The precise geometry that makes a precision connector's high performance possible can be disturbed by dirt and other contamination adhering to connector interfaces. When not in use, keep the connectors covered.

Visual Inspection

Precision connectors should be inspected periodically. Check for the following:

- Bent or broken center pin
- Damaged threads
- Other bent or damaged connector parts
- Dirt or foreign material in connector cavity.

A-3 *REPAIR/MAINTENANCE*

Anritsu recommends that no maintenance other than cleaning be attempted by the customer. Any device with a suspected defective connector should be returned to Anritsu for repair and/or service when needed.

Appendix B
Lightning 37000D
Technical Data Sheet

The latest version of the Lightning 37000D Vector Network Analyzers Technical Data Sheet, Anritsu part number 11410-00350, can be downloaded from from the Anritsu Internet site:

http://www.us.anritsu.com/

This data sheet provides performance specifications for all of the various models in the series.

Appendix C ME7808B/C Technical Data Sheet

The latest version of the ME7808B Technical Data Sheet, Anritsu part number 11410-00330, and ME7808C Technical Data Sheet, Anritsu part number 11410-00410 can be downloaded from from the Anritsu Internet site:

http://www.us.anritsu.com/

Appendix D
ME7808B/C Broadband Measurement System Maintenance

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Appendix D ME7808B/C Broadband Measurement System Maintenance

D-1 INTRODUCTION

This appendix provides maintenance instructions for the ME7808B/C Broadband Measurement system. It describes Maintenance and Performance Verification of the ME7808B/C system. This maintenance and verification is performed independently of any wafer-probe station.

The instruments and components used in the system may vary considerably. The system may be configured with any 37XXXD VNA, 374X Millimeter Wave Modules, with or without Multiplexing Couplers. Many different models of Multiplexing Couplers are designed for use with the ME7808B/C systems Multiplexing Couplers. This appendix covers only the most common system that is configured with 3742A-EW modules and the 37X97D VNA (identified as Configuration 1 in Anritsu literature). Operational and Maintenance information for other system configurations is very similar in many respects. Details on these systems (Configuration 2) can be obtained by contacting your local Anritsu Service Center or the factory.

D-2 MG369XX SYNTHESIZER OPTIONS

The MG369XX series synthesizers used in the ME7808B/C systems may be either of the "A" or "B" families. To meet the System Dynamic Range specifications, Option 3 is required in all synthesizers. The synthesizer used in the LO position must have Option 15X installed if the synthesizer is of the "A" family. If the LO synthesizer is of the "B" family, Option 15X is not required.

D-3 SYSTEM DESCRIPTION

Figure D-3 (next page) shows the functional block diagram of the entire ME7808B/C system (excluding probe station). See Section D-8, Troubleshooting for more detailed information.

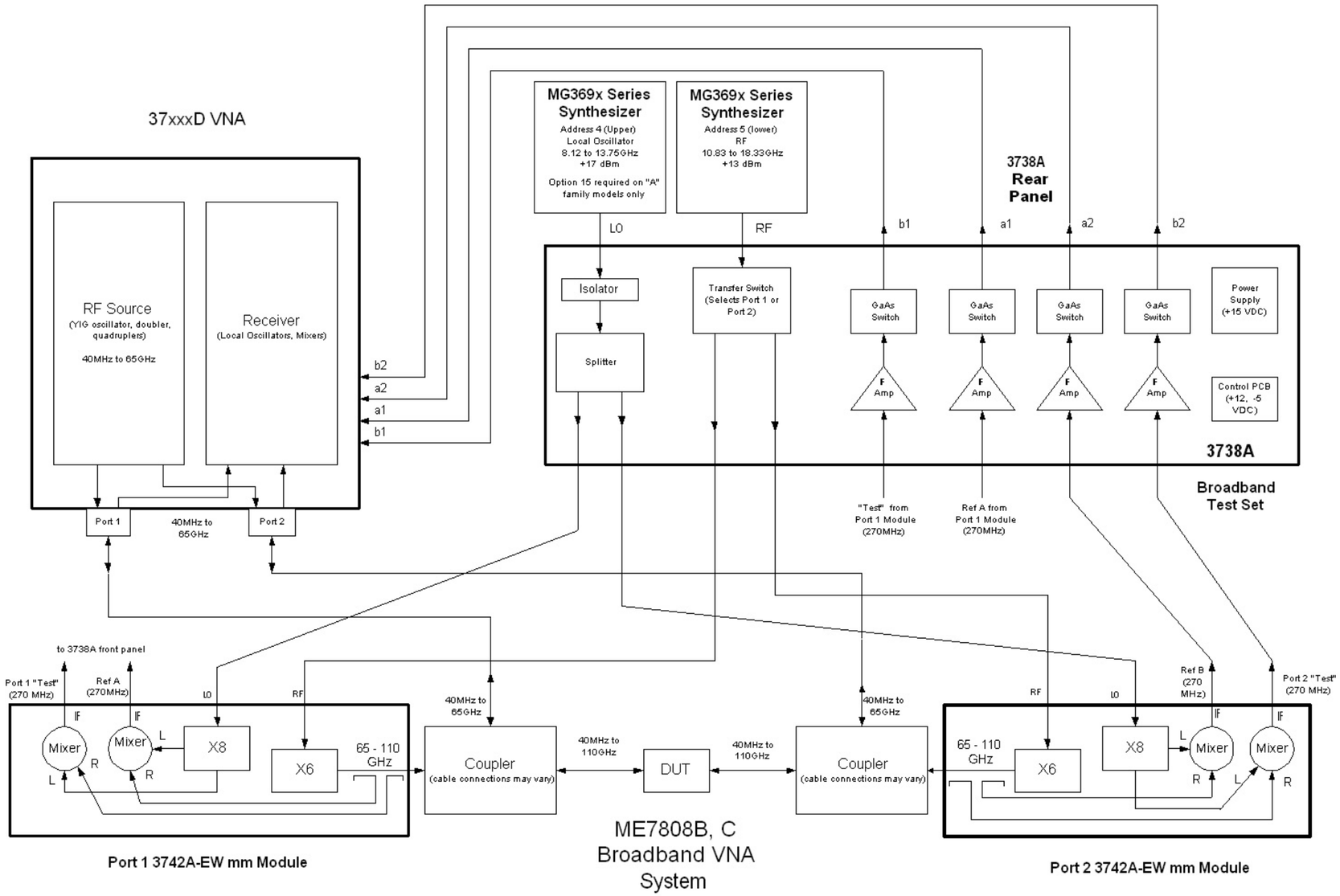


Figure D-1. *ME7808B/C Block Diagram*

D-4 SYSTEM ADJUSTMENTS

Anritsu recommends that the system be readjusted and the performance be verified every 12 months. The 37XXXD instrument and the Synthesizers require adjustment (recalibration). The 3742A modules and the 3738A Test Set are not adjustable.

The 37XXXD instrument adjustments are performed with the system operating in the Internal mode (accessed from the front panel via: Options Menu / Diagnostics / Test Set Config / Internal). Refer to Chapter 6 of this manual for complete instructions on readjustment of the 37XXXD instrument.

For adjustment and verification of the MG369XA synthesizer, refer to the MG369XA Maintenance Manual (part number 10370-10355).

For adjustment and verification of the MG369XB synthesizer, refer to the MG369XB Maintenance Manual (part number 10370-10367).

D-5 REPLACEABLE ITEMS

Part numbers and descriptions of ME7808B/C replaceable system cables and parts and shown in Tables D-1 and D-2. Replacement parts and subassemblies for the 37XXXD VNA are shown in Chapter 2 of this manual. Replacement parts and subassemblies for the MG3690 series synthesizers are shown in the applicable synthesizer maintenance manual.

> ***NOTE***
> There are no serviceable components or subassemblies in the 3742A modules or in the couplers. These items must be returned to Anritsu Customer Service for repair or replacement.

Table D-1. *System Cables*

Description	Part Number
RF Cable, Coupler to 37XXXD	806-101 (ME7808B) or 806-158 (ME7808C)
Cable Set, rear panel, 37XXXD	ND58267
Cable Set, 3742A to 3738A	ND58268
Cable, GPIB	2100-2
RF Cable, Ruggedized, Synthesizer to 3738A LO IN	C34429-7
RF Cable, Ruggedized, Synthesizer to 3738A RF IN	C34429-8

Table D-2. *Model 3738A Replaceable Parts*

Description	Part Number
Power Supply (+15VDC)	40-130
Fan Assembly	ND58282
IF Amplifiers	60-279
IF Switches	1020-44
Isolator	1000-49
RF Splitter	1091-87
PCB Assembly	54074-3
Transfer Switch	ND57971

D-6 PERFORMANCE AND OPERATIONAL TESTS

This chapter describes a series of manually performed tests that will ensure that the system meets many factory specifications. Many of these tests are also duplicated in the 2300-178 software package (version 5.00 and above).

All technical specifications (guaranteed and typical) are found in the ME7808B/C Technical Data Sheet, part numbers 11410-00330 and 11410-00410, found in Appendix C.

Two automated methods are also available for S-parameter measurement accuracy testing (Performance Verification). The test port type being utilized will determine which method is appropriate.

> ***NOTE***
> Anritsu does not support tests or verification processes for wafer probe equipment. Contact the vendor of the wafer probe equipment if such support is desired.

For systems using the W1 coaxial test ports (Multiplexing Couplers of all models), performance verification of the system is accomplished by use of the Anritsu Model 3656 calibration/verification kit and the 2300-496 software (packaged with the kit). This series of automated tests will verify that the system S-parameter measurement accuracy meets factory specifications. Instructions are packaged within the software as an Adobe Acrobat file.

For systems using only WR10 waveguide test ports, NIST traceable verification of S-parameter measurement accuracy may be performed for the system (including a WR10 calibration kit). Contact Anritsu Customer Service in Morgan Hill, California for information about this service.

The balance of this section is dedicated to operational performance tests of the complete ME7808B/C system.

Required Equipment for ME7808B/C System Performance Tests:

- PC with Windows 95 or equivalent operating system
- National Instruments GPIB hardware and software installed in the PC
- Anritsu 2300-178 (3700TEST) Software Version 5.00 Minimum
- Anritsu 3654B Calibration Kit
- Anritsu 3670V50-2 RF Cable (Throughline)
- Anritsu 3655W (WR10) Calibration Kit or
  Maury Z7005G19 (WR10) Calibration Kit

Optional Equipment:

- HP Model 432A Power Meter with power sensor(s) covering 65 to 110 GHz
- Voltmeter (for troubleshooting only)
- Anritsu ML24XX Power Meter with 20 GHz Power Sensor (for troubleshooting only)

Preliminary:

Step 1. Move millimeter modules and cables to another location so that the PC keyboard and the 37XXXD front panel are easily accessible.

Step 2. Press the Option Menu key.

Step 3. Select **TEST SET CONFIG / INTERNAL**, then press <Enter> to accept.

Step 4. On the rear panel of the 37XXXD, remove the cable set which connects to the 3738A, and install the small terminations (hanging from the chains) to the SMA connectors on the back of the 37XXXD .

Step 5. If not already completed, perform the tests described in Section 4-4 to ensure that the 37XXXD is operating normally. It is not necessary to perform the 12-Term Cal Test or subsequent tests.

Synthesizer Verification:

Refer to the appropriate Maintenance Manual for the synthesizers installed in the system for detailed Verification instructions. No further checks are necessary in the ME7808B/C system.

3742A-EW Operational Performance Tests:

Most specifications for the system when operating from 65 to 110 GHz are not published (guaranteed) but are typical values. Systems which pass the following tests are operating in the expected manner and are capable of making accurate measurements.

Assemble the complete system with the 3742A modules installed, with all front and rear panel cables reconnected. Then perform the following steps.

Step 1. Configure system as a 65-110 GHz system. To do this, press the Utility Menu and select **TEST SET CONFIG / MILLIMETER WAVE** and press the <Enter> key. Select the WR-10 Extended band.

Step 2. Set the power vernier knobs on the 3742A modules fully CW to set maximum power at the test ports.

Step 3. In this mode of operation, most tests described below (excluding Directivity and Coupler tests) may be performed using the 2300-178 Test Program.

Step 4. Remove the Couplers from the mmWave modules. Insure the 2 inch gold waveguide sections are installed to the test ports of the mmWave modules.

Step 5. Connect the two modules together.

Step 6. View S21 and S12.

Step 7. Ensure the system sweeps normally in this mode.

Step 8. Ensure both power control knobs on the mmWave modules are functional. It is normal for Lock Failures to appear at lower power. Return power control knobs to maximum power settings.

Step 9. Clear the errors from the Service Log.

IF Power Level Test:

This test verifies that each individual receiver channel operates properly. Measurement calibration of the system is not required for this test. Ensure the system has warmed up for at least 1 hour before performing this test.

Step 1. Install a flush short on the test port of the Port 1 mmWave module.

Step 2. Set up the network analyzer as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 1
	User Ratio: a1/1
	User Phase Lock: a1
	Channel 3
	User Ratio: b1/1
	User Phase Lock: a1
SET SCALE	Resolution: 10 dB/Div (both channels)
	Reference Value: -10 dB
LIMITS	Channel 1 (a1/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-28 dB)
	Channel 3 (b1/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-38 dB)

Step 3. Ensure that the displays for Channels 1 and 3 fall between the limit lines, and that no error messages appear on the display.

Step 4. Install a flush short to the Port 2 mmWave module.

Step 5. Set up the network analyzer as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 2 & 4
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 2
	User Ratio: a2/1
	User Phase Lock: a2
	Channel 4
	User Ratio: b2/1
	User Phase Lock: a2
SET SCALE	Resolution: 10 dB/Div (both channels)
	Reference Value: -10 dB
LIMITS	Channel 2 (a2/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-28 dB)
	Channel 4 (b2/1)
	Upper Limit: ON (-1 dB)
	Lower Limit: ON (-38 dB)

Step 6. Ensure that the displays for Channels 2 and 4 fall between the limit lines, and that no error messages appear on the display.

Test Port Power Test:

Step 1. Default the system (Press Default Program key two times). Display Single Channel, S11.

Step 2. Connect the HP432A Power Meter and sensor to the Port 1 mmWave module test port.

Step 3. For each frequency on the power sensor, read the power at the Port 1. The power should be 0 to -10 dBm for each frequency.

Step 4. Display Single Channel, S22. Connect the power sensor to Port 2. Repeat steps 2 and 3 for the Port 2 module.

Performance Verification- High Level Noise (Reflection) Test:

The following test verifies that the high level noise in the system will not significantly affect the accuracy of subsequent measurements. High level noise is the random noise that exists in the system, and cannot be accurately predicted or measured, thus it cannot be removed by conventional error-correction techniques. Measurement calibration is not required for these tests. Ensure the system has warmed up for at least 1 hour before performing this test.

Step 1. Connect flush shorts to both test ports of the mmWave modules.

Step 2. Default the system (press DEFAULT PROGRAM two times).

Step 3. Set the system as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 1: S11
	Channel 3: S22
SET SCALE	Resolution: 0.05 dB/division (both channels)
LIMITS	Channel 1
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)
	Channel 3
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)

Step 4. Be careful not to bump any system components (especially cables) during this test. Select Channel 1. After several sweeps, press TRACE MEMORY, and select Store Data to Memory. Select View Data/Memory.

Step 5. Be sure the RF display remains between the limit lines for approximately 5 sweeps. (It is normal for the data to drift out of the limit lines after a short period of time).

Step 6. Repeat steps 4 and 5 for Channel 3.

Performance Verification—High Level Noise (Transmission) Test:

The following test verifies that the high level noise in the system will not significantly affect the accuracy of subsequent measurements. High level noise is the random noise that exists in the system. It cannot be accurately predicted or measured, thus it cannot be removed by conventional error-correction techniques. Measurement calibration is not required for these tests. Ensure the system has warmed up for at least 1 hour before performing this test.

Step 1. Remove the flush shorts and connect the mmWave modules together.

Step 2. Set the system as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz
	Stop: 110 GHz
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both channels)
S PARAMS	Channel 1: S12
	Channel 3: S21
SET SCALE	Resolution: 0.05 dB/division (both channels)
LIMITS	Channel 1
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)
	Channel 3
	Upper Limit: ON (0.04 dB)
	Lower Limit: ON (-0.04 dB)

Step 3. Be careful not to bump any system components (especially cables) during this test. Select Channel 1.

Step 4. After several sweeps, press TRACE MEMORY, and select Store Data to Memory. Select View Data/Memory.

Step 5. Be sure the RF display remains between the limit lines for approximately 5 sweeps. (It is normal for the data to drift out of the limit lines after a short period of time).

Step 6. Repeat steps 3 and 4 for Channel 3.

Drift Test:

Step 1. Leave the equipment connected as described in the previous test (High Level Noise Transmission). Ensure the system has warmed up for 2 hours.

Step 2. Change Graph Type to Log Mag and Phase for both channels.

Step 3. Store Data to Memory and View Data/Memory for both channels.

> ***CAUTION***
>
> Do not move any part of the system after this point. Be especially careful to not bump the cables.

Step 4. At the end of 1/2 hours, Autoscale both channels.

Step 5. Set Limit Lines to +/- 0.2 dB, and +/- 2 Degrees for both channels. Ensure displays fall within the limit lines.

Performance Verification—12 Term OSL Calibration:

This calibration is required to perform the System Dynamic Range, Source Match, and Directivity tests. Ensure the system has warmed up for at least 1 hour before performing this test, and that the precision 2 inch waveguide sections are installed to the test ports of the mmWave modules.

Step 1. Insert the Calibration Coefficient disk from the WR-10 calibration kit into the floppy drive of the 37XXXD and load the coefficients via the UTILITY MENU key.

Step 2. Press BEGIN CAL.

Step 3. Make the following selections from the menus to perform a full band 12 Term Calibration:

- ❑ Change Cal Method and Line Type
- ❑ Waveguide
- ❑ Full 12 Term
- ❑ Include Isolation (required for System Dynamic Range test)
- ❑ Sliding Load (required for Directivity and Source Match tests)
- ❑ Use Installed Kit

Step 4. Before measuring the Isolation Devices (terminations), make the following changes to the setup:

- ❑ AVERAGE/SMOOTH MENU key: Change to 512 averages
- ❑ IFBW key: Change to Minimum (10 Hz)
- ❑ Measure the Isolation Devices.

Step 5. Finish the calibration using the instructions on the VNA display.

Performance Verification—Source Match and Directivity Tests:

Ensure the 12 Term Calibration was performed as described above (sliding loads were used) and the calibration is active (APPLY CAL LED is ON). During this test, do not disconnect the gold waveguide sections which were used during the 12 Term Calibration.

Source Match Test:

Step 1. Set up system as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz Stop: 110 GHz
CHANNEL MENU	Single Channel Channel 1
GRAPH TYPE	Log Magnitude
SET SCALE	Resolution: 0.1 dB/DIV Ref Value: 0.0 dB Reference Line: TOP
S-PARAMS	S11

Step 2. Attach a second high-precision waveguide section to the module on Port 1.

Step 3. Attach a flush short to the end of the high-precision waveguide section.

Step 4. While observing the sweep indicator, allow at least one complete sweep to occur. Press Autoscale to center the trace.

Step 5. Press Marker Menu, and select MARKER 1, MARKER 2, and MARKER 3, to be ON.

Step 6. Using the rotary knob, position marker 1 and marker 2 to adjacent peaks of the ripple with the greatest negative trough (or adjacent troughs if the ripple has the greatest positive peak); position marker 3 to the bottom of the trough (or the top of the peak if the ripple has the greatest positive peak). Refer to Figure D-3 (following page).

Step 7. Using the Marker Menu and Readout Marker key menus, record the absolute value of markers 1 and 2 as follows:

- Subtract one from the other.
- Halve the difference
- Add the resultant to the value of the marker at the lowest peak (or the deepest trough).

This is the average value of the two peaks (or troughs).

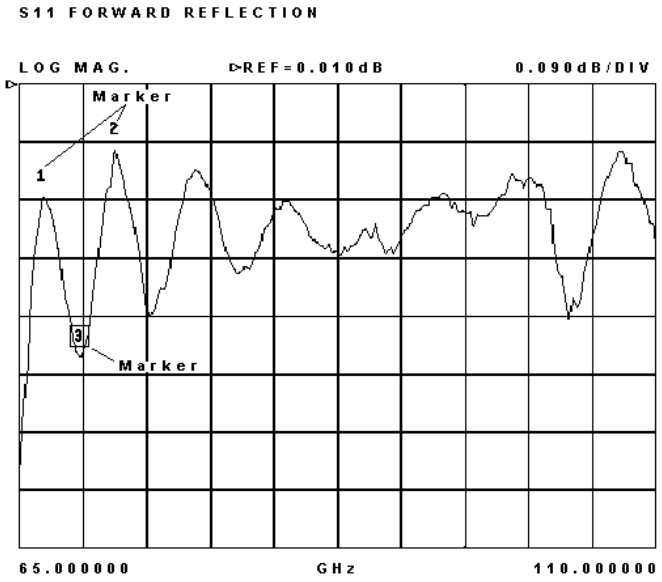


Figure D-2. *Markers*

Step 8. Record the marker 3 value.

Step 9. Find the absolute difference of the values recorded in step 7 and step 8. This is the Peak-to-Peak Ripple value. Use the RF Measurement Chart (Table D-3) to find the corresponding Return Loss value. This value is the Effective Source Match. Insure Source Match measures at least 30 dB.

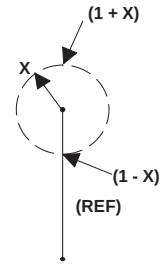
Step 10. Change the S Parameter to S22. Move the outside waveguide section with the short attached to the Port 2 module.

Step 11. Repeat Steps 4 through 9 to compute Port 2 Source Match. Verify Port 2 Source Match is 30 dB minimum.

Table D-3. *Microwave Measurement Chart*

IMPORTANT NOTE

Conversion tables for Return Loss, Reflection Coefficient, and SWR with tabular values for interaction of a small phasor x with a large phasor (unity reference) expressed in dB related to reference.



PHASOR INTERACTION

TERM002.DRW

			Relative to Unity Reference			
SWR	Reflection Coefficient	Return Loss (dB)	X dB Below Reference	REF + X dB	REF – X dB	REF / X Peak to Peak Ripple dB
17.3910	0.8913	1	1	5.5350	–19.2715	24.8065
8.7242	0.7943	2	2	5.0780	–13.7365	18.8145
5.8480	0.7079	3	3	4.6495	–10.6907	15.3402
4.4194	0.6310	4	4	4.2489	–8.6585	12.9073
3.5698	0.5623	5	5	3.8755	–7.1773	11.0528
3.0095	0.5012	6	6	3.5287	–6.0412	9.5699
2.6146	0.4467	7	7	3.2075	–5.1405	8.3480
2.3229	0.3981	8	8	2.9108	–4.4096	7.3204
2.0999	0.3548	9	9	2.6376	–3.8063	6.4439
1.9250	0.3162	10	10	2.3866	–3.3018	5.6884
1.7849	0.2818	11	11	2.1567	–2.8756	5.0322
1.6709	0.2512	12	12	1.9465	–2.5126	4.4590
1.5769	0.2239	13	13	1.7547	–2.2013	3.9561
1.4985	0.1995	14	14	1.5802	–1.9331	3.5133
1.4326	0.1778	15	15	1.4216	–1.7007	3.1224
1.3767	0.1585	16	16	1.2778	–1.4988	2.7766
1.3290	0.1413	17	17	1.1476	–1.3227	2.4703
1.2880	0.1259	18	18	1.0299	–1.1687	2.1986
1.2528	0.1122	19	19	0.9237	–1.0337	1.9574
1.2222	0.1000	20	20	0.8279	–0.9151	1.7430
1.1957	0.0891	21	21	0.7416	–0.8108	1.5524
1.1726	0.0794	22	22	0.6639	–0.7189	1.3828
1.1524	0.0708	23	23	0.5941	–0.6378	1.2319
1.1347	0.0631	24	24	0.5314	–0.5661	1.0975
1.1192	0.0562	25	25	0.4752	–0.5027	0.9779
1.1055	0.0501	26	26	0.4248	–0.4466	0.8714
1.0935	0.0447	27	27	0.3796	–0.3969	0.7765
1.0829	0.0398	28	28	0.3391	–0.3529	0.6919
1.0736	0.0355	29	29	0.3028	–0.3138	0.6166
1.0653	0.0316	30	30	0.2704	–0.2791	0.5495
1.0580	0.0282	31	31	0.2414	–0.2483	0.4897
1.0515	0.0251	32	32	0.2155	–0.2210	0.4365
1.0458	0.0224	33	33	0.1923	–0.1967	0.3890
1.0407	0.0200	34	34	0.1716	–0.1751	0.3467
1.0362	0.0178	35	35	0.1531	–0.1558	0.3090
1.0322	0.0158	36	36	0.1366	–0.1388	0.2753
1.0287	0.0141	37	37	0.1218	–0.1236	0.2454
1.0255	0.0126	38	38	0.1087	–0.1100	0.2187
1.0227	0.0112	39	39	0.0969	–0.0980	0.1949
1.0202	0.0100	40	40	0.0864	–0.0873	0.1737
1.0180	0.0089	41	41	0.0771	–0.0778	0.1548
1.0160	0.0079	42	42	0.0687	–0.0693	0.1380
1.0143	0.0071	43	43	0.0613	–0.0617	0.1230
1.0127	0.0063	44	44	0.0546	–0.0550	0.1096
1.0113	0.0056	45	45	0.0487	–0.0490	0.0977
1.0101	0.0050	46	46	0.0434	–0.0436	0.0871
1.0090	0.0045	47	47	0.0387	–0.0389	0.0776
1.0080	0.0040	48	48	0.0345	–0.0346	0.0692
1.0071	0.0035	49	49	0.0308	–0.0309	0.0616
1.0063	0.0032	50	50	0.0274	–0.0275	0.0549
1.0057	0.0028	51	51	0.0244	–0.0245	0.0490
1.0050	0.0025	52	52	0.0218	–0.0218	0.0436
1.0045	0.0022	53	53	0.0194	–0.0195	0.0389
1.0040	0.0020	54	54	0.0173	–0.0173	0.0347
1.0036	0.0018	55	55	0.0154	–0.0155	0.0309
1.0032	0.0016	56	56	0.0138	–0.0138	0.0275
1.0028	0.0014	57	57	0.0123	–0.0123	0.0245
1.0025	0.0013	58	58	0.0109	–0.0109	0.0219
1.0022	0.0011	59	59	0.0097	–0.0098	0.0195
1.0020	0.0010	60	60	0.0087	–0.0087	0.0174

Effective Directivity Test:

Step 1. Remove the flush short from the end of the high-precision waveguide section. Point the test ports away from all reflective objects.

Step 2. Press Autoscale key to center the trace.

Step 3. Repeat step 6 through 8.

Step 4. Find the absolute difference of the values recorded in step 7 and step 8. This is the Peak-to-Peak Ripple value. Use the RF Measurement Chart to find the corresponding Return Loss value.

Step 5. Find the corresponding REF + X or REF - X value from the RF Measurement Chart. Use the following formula to calculate the effective directivity value:

For ripple with negative trough:

Effective Directivity =
Return Loss value + (Absolute Value of Marker 3)-(REF - X)

For ripple with positive peak:

Effective Directivity =
Return Loss value +(Absolute Value of Marker 3)+(REF + X)

Step 6. Verify the Effective Directivity is >35 dB from 65 to 75 GHz, and >40 dB from 75 to 110 GHz.

Step 7. Change the S Parameter back to S11, and move the outside waveguide section back to the Port 1 module.

Step 8. After 2 sweeps, press AUTOSCALE.

Step 9. Repeat steps 4, 5 and 6 to calculate Port 1 Directivity. Verify the Effective Directivity is >35 dB from 65 to 75 GHz, and >40 dB from 75 to 110 GHz.

Performance Verification—System Dynamic Range:

System Dynamic Range is defined as the ratio of the typical power at Port 1 and the System Noise Floor. A 12 Term Calibration (performed exactly as described in this Appendix) must be activated. *Video IF Bandwidth and Averaging must be set as shown in the chart below.*

Step 1. Attach a broadband termination to both test ports of the 3742A mmWave modules.

Step 2. Set up the VNA display as shown below:

Key	Menu Choice
SETUP MENU	Start: 65 GHz Stop: 110 GHz CW Mode: ON
CHANNEL MENU	Dual Channels 1 & 3
GRAPH TYPE	Log Magnitude (both Channels)
SET SCALE	Resolution: 10 dB/division Reference Value: -50 dB Reference Line: 7
S-PARAMS	Channel 1: S12 Channel 3: S21
DATA POINTS	401
VIDEO IFBW	10 Hz (Minimum)
AVG/SMOOTH MENU	512 Averages (ON)
LIMITS:	Lower Limit ON (see chart below, both channels)
DATA POINTS	50 Points in CW

Step 3. Allow the system to sweep both forward and reverse. Ensure the data does not go above the limit line on either channel. Check each frequency in the chart below.

CW Freq (GHz)	Specification (dB)
65	79
75	90
85	90
100	87
110	82

D-7 MULTIPLEXING COUPLER CHECK

This test checks the insertion loss of many models of couplers. Only coupler models that employ one cable to the 37000D Port 1 and Port 2 can be tested using this method. Couplers that employ multiple cables to the 37000D Option 15 connectors must be tested using the 3656 Calibration/Verification Kit with its associated software.

Equipment Required:

- Anritsu 3656 Calibration/Verification Kit
- Anritsu 3654B Calibration Kit
- Anritsu 3670V50-2 Test Port Cables (Two each)
- Anritsu 3655W Cal Kit or Maury Microwave Model Z7005G19 WR-10 Waveguide Calibration Kit

Coupler Low Frequency Test (Coaxial—V Connector):

Step 1. Remove the multiplexing Couplers from the mmWave modules and use the 33WFWF50 adapter from the 3656 cal kit to connect the W1(m) connectors of the Couplers together.

Step 2. Remove the mmWave modules from the test area and set the 37XXXD Test Set Configuration (Option Menu key) to Internal

Step 3. Set up the VNA as shown in the table below:

Key	Menu Choice
SETUP MENU	Start: 40 GHz Stop: 65 GHz
CHANNEL MENU	Single Channel: Channel 3
GRAPH TYPE	Log Magnitude
SET SCALE	Resolution: 10 dB/division Reference Value: 0 dB Reference Line: 8
S-PARAMS	S21

Step 4. Attach the throughlines to the VNA (Port 1 and Port 2). Use the 3654B Calibration Kit to perform a 12 Term calibration at the ends of the throughlines.

Step 5. Leave the waveguide ports of the couplers open, attach the couplers between the throughlines, then measure the S21 insertion loss of the couplers.

Step 6. Verify that the insertion loss is less than 15 dB and there are no sharp discontinuities.

Coupler High Frequency Test (Waveguide—WR10):

Step 1. Reconnect the 3742A-EW mmWave modules to the system and set the Test Set Configuration to the 3742A-EW Millimeter (or Broadband) mode.

Step 2. Set the VNA as shown below.

Key	Menu Choice
SETUP MENU	Start: 65 GHz Stop: 110 GHz
CHANNEL MENU	Single Channel: Channel 3
GRAPH TYPE	Log Magnitude
SET SCALE	Resolution: 10 dB/division Reference Value: 0 dB Reference Line: 8
S-PARAMS	S21

Step 3. Use the WR-10 Waveguide Calibration Kit to perform a 12-Term Broadband Load calibration.

Step 4. Connect coupler pair between the two mmWave modules. The V(f) connectors of the couplers need to be terminated with the 28V50B terminations from the 3654B Calibration Kit.

Step 5. Verify that the insertion loss is less than 20 dB and there are no sharp discontinuities.

D-8 TROUBLESHOOTING

Troubleshooting this system is accomplished by first ensuring no set-up error exists, then determining which instrument has failed.

Front Panel and Cabling Checks:

Step 1. Ensure the following:

- ❑ The power control knobs on the top of the 3742A modules are set fully CW.
- ❑ No error messages are shown on the front panels of the synthesizers.
- ❑ The top synthesizer is GPIB address 4, and it has Option 15A installed (Option 15 is not required on B series snthesizers).
- ❑ The lower synthesizer is GPIB address 5.
- ❑ All cables are on securely and are connected to the right positions.

Step 2. Press the Utility Menu key, then select **DISPLAY INSTRUMENT PARAMETERS / SYSTEM** and ensure that both synthesizers are shown.

General Troubleshooting of the System:

Step 1. After determining that the problem is not caused by cabling, synthesizer, or GPIB setup errors, isolate the problem instrument using the a process of elimination. The critical information to know is direction (only forward, only reverse, or both) and frequency (all frequencies, or only below 38 GHz, only from 38 GHz to 65 GHz, or only above 65 GHz).

Step 2. To determine direction, be sure to display only one channel at a time.

Step 3. If the problem occurs at any frequency below 65 GHz, you can assume the fault lies in the 37XXXD. Refer to Chapter 7 for troubleshooting help on this instrument.

Step 4. If the problem occurs in only one direction (forward or reverse), you can eliminate both synthesizers as cause.

Step 5. If the problem is only in one direction, and only above 65 GHz, the problem is in the 3742A or the 3738A test set or 37XXXD.

Step 6. If you swap the 3742A's, and the problem moves, one 3742A is defective. If you swap the 3742A's and the problem does not move, the failure is in the 3738A or the 37XXXD.

3738A Checks:

Step 1. If it is possible that the 3738A is defective, ensure the system is in the Millimeter Mode (not Broadband or Internal), remove the cover of the 3738A and make the checks described below to verify proper operation.

Step 2. Note that many DC voltages will change as the system changes between forward and reverse measurement, so be sure to set the system as indicated.

DC Power Supplies and General PCB Tests:

On the following test points of the 54074-3 PC board, verify the following DC voltages from TP8 ground (+/- approximately 10%). All supplies except the TP5 voltage are derived from regulators found on the PCB.

- TP5: +15 VDC (provides power for all other DC supplies*)
- TP3: +12 VDC (IF Amp bias)
- TP4: +5VDC (for PCB internal circuits)
- TP6: +5 VDC (not used)
- TP7: +12VDC (fan power)
- TP11: –5VDC (not used)

* If TP5 has an incorrect voltage, replace the power supply with the part number shown on Table D-2.

PCB Control Signals:

Step 1. With the system still in the Millimeter mode, set the instrument to display Single Channel, S21. Make the following checks, and note the probable failed part. Be sure to use the sequence shown below when diagnosing and determining which part to replace.

Location	Required Signal	Replace if Required Signal Fails
TP 14	TTL low	37XXXD A8 PCB
TP 9	–5V	37XXXD A8 PCB or 3738A control PCB
TP 10	0V	37XXXD A8 PCB or 3738A control PCB
Port 1 LED	ON	*Port 1 LED
TP 1	+12 VDC	Entire PCB
TP 2	0 VDC	Entire PCB
J9 pin 1 on PCB	~ -3.8 VDC	Entire PCB or transfer switch
J9 pin 2 on PCB	~ +2.2 VDC	Entire PCB or transfer switch

*Note that if the LED fails, the PCB will not operate, and forward only will fail.

Step 2. Set the instrument to display Single Channel, S12. Make the following checks on the 54074-3 PCB, and note the probable failed part. Be sure to use the sequence shown below when diagnosing and determining which part to replace.

Location	Required Signal	Replace if Required Signal Fails
TP 14	TTL low	37XXXD A8 PCB
TP 9	–5V	37XXXD A8 PCB or 3738A control PCB
TP 10	0V	37XXXD A8 PCB or 3738A control PCB
Port 2 LED	ON	*Port 2 LED
TP1	0 VDC	Entire PCB
TP2	+12 VDC	Entire PCB
J9 pin 1 on PCB	~ +2.2 VDC	Entire PCB or transfer switch
J9 pin 2 on PCB	~ –3.8 VDC	Entire PCB or transfer switch

*Note that if the LED fails, the PCB will not operate, and reverse only will fail.

3738A LO Path:

As shown in Figure D-3, there are no switching or active components in this signal path once the signal has left the synthesizer. Inside the 3738A, the signal from the synthesizer is routed through an isolator, through a splitter, and then out the Port 1 and Port 2 LO connectors for use by the modules.

The total insertion loss through the 3738A is about 5 dB, therefore the power out of the front panel Port 1 and Port 2 LO connectors should measure approximately +11 dBm, regardless of sweep direction. Use the ML24xx Power Meter to verify this power.

3738A RF Path Description and Checks:

As shown in Figure D-3, a transfer switch controls the presence of RF signal at the 3738A RF OUT ports. If the VNA is making a forward measurement, approximately +11 dBm is present at the Port 1 RF OUT. If the measurement is reverse, the same power is present only at the Port 2 RF OUT. Use the ML24xx Power Meter to verify this power.

3738A IF Path Description and Checks:

As shown in Figure D-3, there are four separate IF paths in the 3738A. Each path is composed of an ampifier (gain is approximately 13 dB) and a GaAs switch. The signal through these paths is fixed at 270 MHz, which is the down-converted signal from the 3742A modules.

Regardless of sweep direction, the GaAs switches and the IF amplifiers are biased ON (pass RF) when the system frequency is above 65 GHz, and are OFF when the system frequency is below 65 GHz. Correct bias voltages at TP3, TP9, and TP10 are shown on the chart above.

System Dynamic Range Problem:

Ensure that both MG369XX synthesizers have Option 3 installed and that the IF Power Level tests pass.

RF Overload Messages Appear:

This may be caused by the 374XA modules being moved from one ME7808B/C system to another due to normal variations in amplifier gains between different systems. To solve the problem, install a 3 dB pad between the 37XXXD rear panel and the appropriate RF cable (a1, a2, b1, b2).

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